YASKAWA ELECTRIC

SIE-C815-13•12
DESCRIPTIVE INFORMATION

PROGRAMMABLE CONTROLLER

Memocon™-SC GL20/GL60S

USER'S MANUAL

PRESET COUNTER MODULE

TYPE JAMSC-B2802

1. INTRODUCTION

The 2000 Series JAMSC-B2802 I/O preset counter module (in this manual, abbreviated to B2802) is a counter incorporating one circuit up to 50kpps, for both A/B phase pulse input and code + pulse input modes.

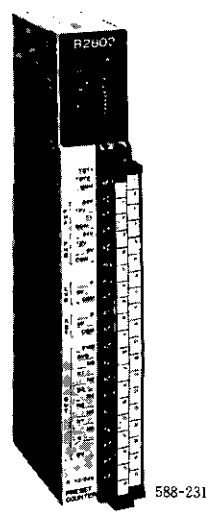
When a notch point set value is preset by the cpu module, B2802 compares all the pulse counts and the notch point set value, and outputs notch signals continuously (9 lines) on the basis of the comparison results.

As a CPU module, both Memocon-SC GL20 (hereinafter, GL20) and Memocon-SC GL60S (herein-after, GL60S) can be used. The main features of B2802 are as follows:

- The notch output is in two patterns; A and B.
- The notch output may be given hysteresis.
- Counting is up to 6-digit decimal (GL20) or 8-digit decimal (GL60S)
- The digit positions can be expanded by carrying and/or borrowing.
- The count can be simply checked by the counting test input.
- The 9 notch outputs can be independently turned on and off, without comparison with the pulse counts.

<REFERENCE>

- SIE-C815-13 . 1: ***Memocon-SC*** **GL20**
  USER'S MANUAL DESIGN AND MAINTENANCE
- SIE-C815-13 . 5: ***Memocon-SC*** **GL20**
  USER'S MANUAL P150 PROGRAMMING PANEL
- SIE-C815-14 . 1: ***Memocon-SC*** **GL60S**
  USER'S MANUAL-No. 1 DESIGN AND MAINTENANCE
- SIE-C815-14 . 2: ***Memocon-SC*** **GL60S**
  USER'S MANUAL-No. 2 BASIC INFORMATION
- SIE-C815-14 . 3: ***Memocon-SC*** **GL60S**
  USER'S MANUAL-No. 3 SFC INFORMATION
- SIE-C815-14 . 7: ***Memocon-SC*** **GL60S**
  REMOTE I/O USER'S MANUAL



Preset Counter Module
Type JAMSC-B2802

NOTE

1. Inquiries about the information in this manual should be directed to your YASKAWA representative.

2. No part of this manual may be reproduced without permission.

CONTENTS

INDEX

2. CONFIGURATION

An example of B2802 system configuration is shown in Fig. 2.1.
(using GL20 for CPU and one B2802 module.)

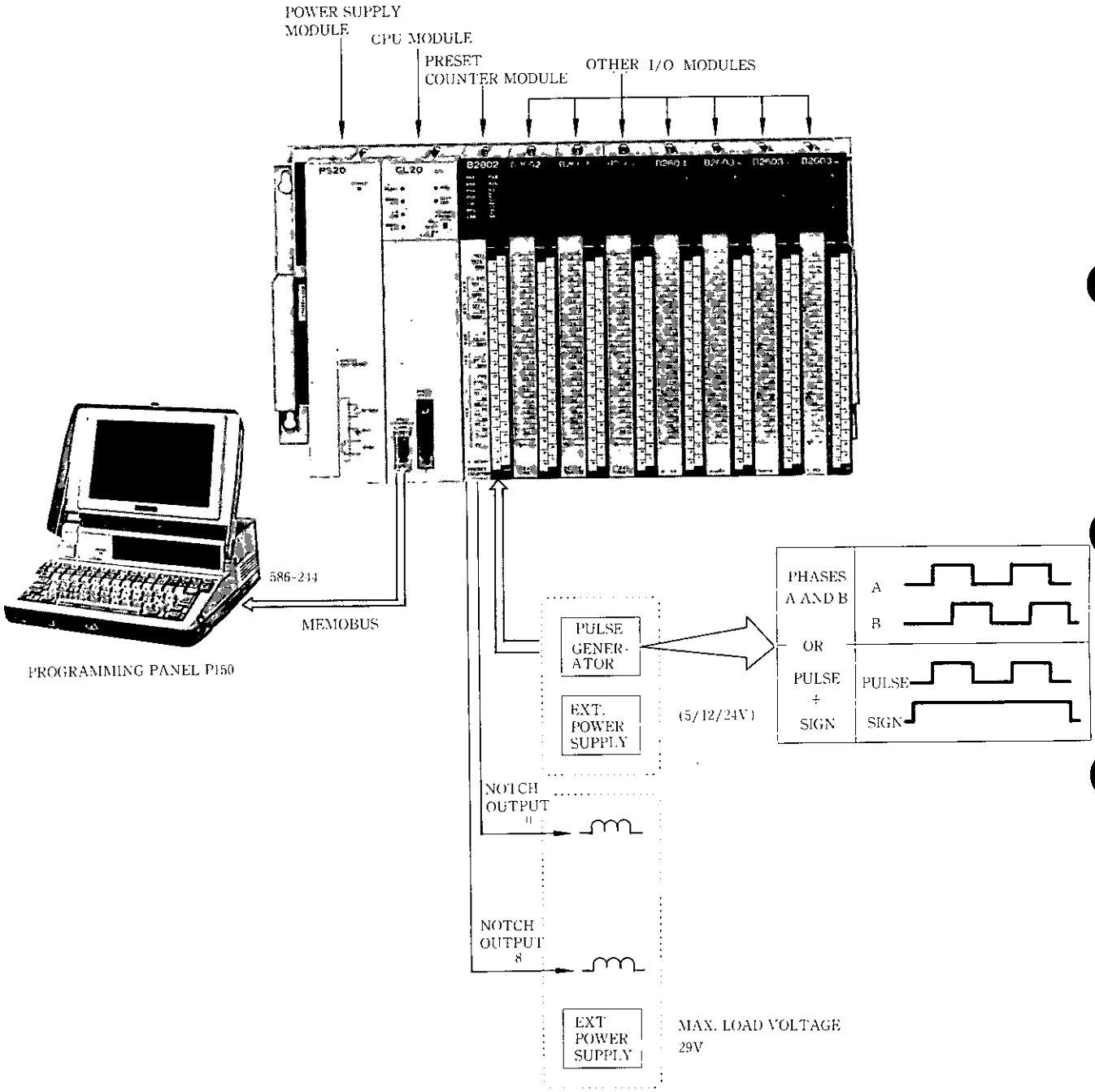


Fig. 2.1 B2802 System Configuration

3. SPECIFICATIONS

3.1 GENERAL SPECIFICATIONS

Table 3.1 General Specifications

Item	Specification
Model	JAMSC - B2802
Ambient Temperature	0 to + 55℃
Storage Temperature	-20 to + 85℃
Humidity	10 to 90% RH (non-condensing)
Vibration Resistance	In compliance with JIS* C0911 (Range: 10 to 55 Hz, amplitude: 0.075mm, No. of sweeps: 10 times)
Shock Resistance	In compliance with JIS* C0912 (10G max.)
Environmental Condition	Free from explosive, inflammable and/or corrosive gases.
Dielectric Strength, Resistance	Strength: 1500 VAC for one minute (Internal circuit against external circuit) Resistance: 500VDC, 100MΩmin.
Noise Resistance	1500V, 1μs, 1ns at startup, by noise simulator
Dimensions in mm (inches)	38(1.50)W×250(9.84)H×104(4.10)D† , 1 Span
Weight	Approximately 0.6kg 1.3lb
Internal Consumable Current (Vcc)	5VDC ± 3% 0.25A

* Japanese Industrial Standard
† Including terminal block

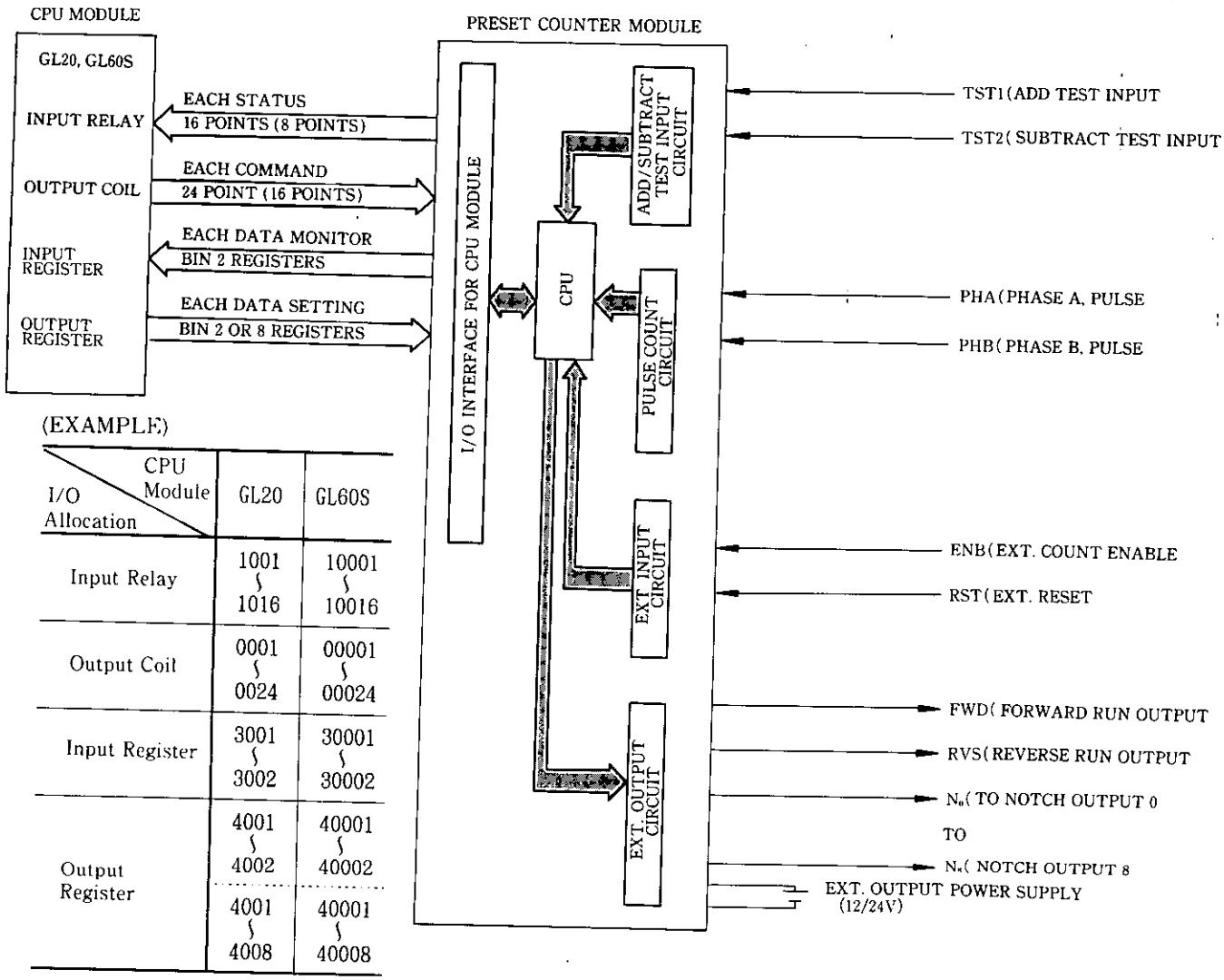
3.2 PERFORMANCE SPECIFICATIONS

Table 3.2 Performance Specifications

Item		Specification	Remarks
Function		Pulse count and output of external notch signal	–
Number of Counter Circuits		One circuit	–
Adaptable CPU Module		GL20, GL60S	Selected by a switch
I/O Allocation, Points/Registers		Input relay : 16 points (also 8 points) Output coil : 24 points (also 16 points) Input register : 2 registers binary allocation Output register : 2 or 8 registers binary allocation	Number of allocations for CPU modules
Count specification	Counter Digits	6-digit decimal (GL20) 8-digit decimal (GL60S)	Selected by a switch
	Maximum Counting Speed	50kpps (Multiplier 1), 100kpps (Multiplier 2), 200kpps (Multiplier 4)	–
	Counting Pulse Method	Phase A/B (Multipliers 1, 2 and 4)sign + pulse (Multiplier 1)	Selected by initial setting
	Pulse Input Voltage	5VDC, 12VDC, 24VDC	Selected by terminal block. Ext. power supply required.
External Input Signal		External count enable, external reset, ADD test, SUBTRACT test	Corresponds to 12 V and 24 V inputs.
External Output Signal		FWD run, RVS run, 9 notches	Open collector output, power supply required.
Monitor Function		Provided.	–
External Power Supply		For pulse input : 5, 12, 24 V For ext. output signal : 12, 24 V	–

3.3 INTERFACE OF CPU MODULE AND EXTERNAL DEVICES

Fig. 3.1 shows the relationship between B2802 interfaces, CPU module (GL20, GL60S), and external devices.



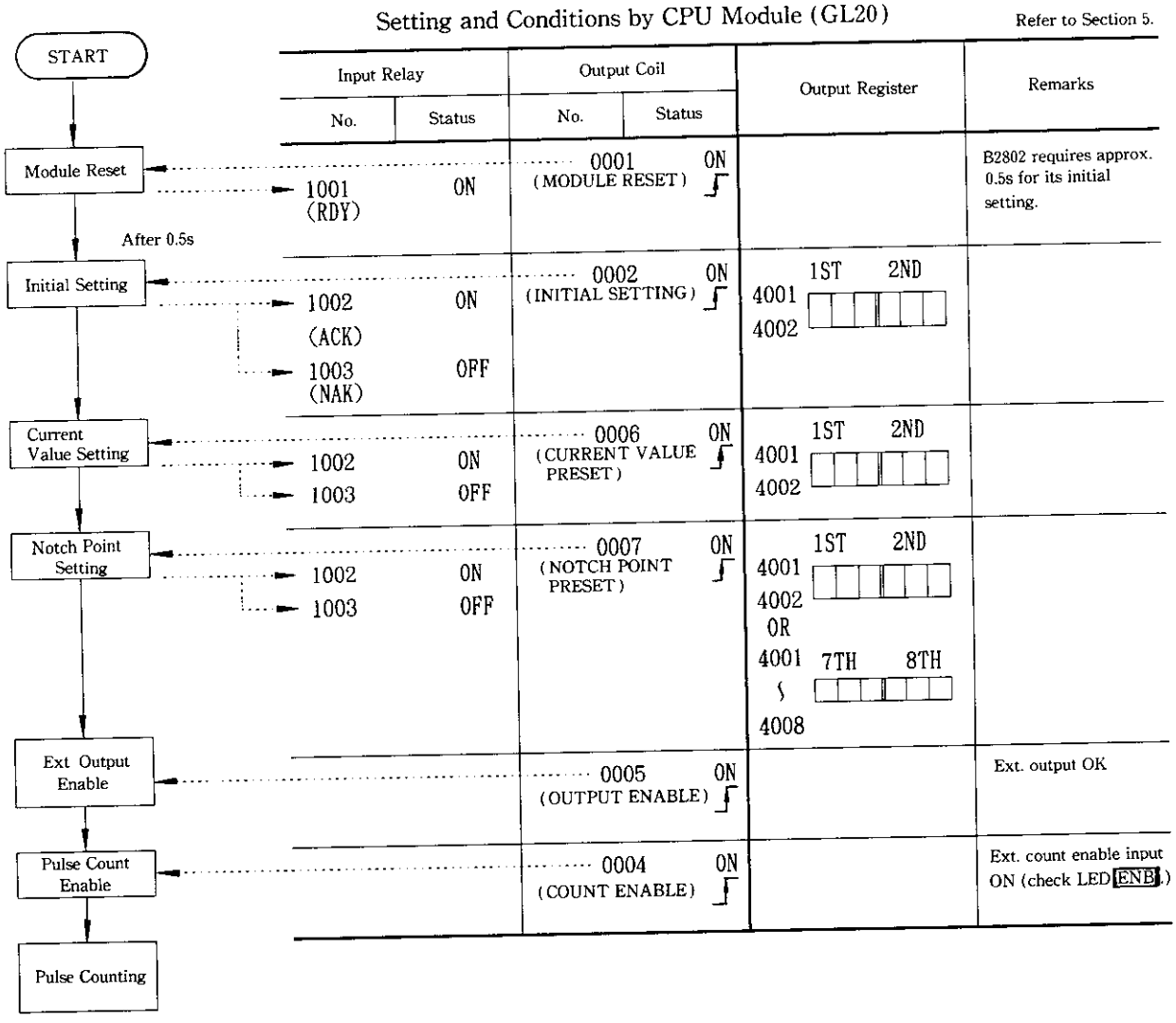
(EXAMPLE)

I/O Allocation \ CPU Module	GL20	GL60S
Input Relay	1001 ~ 1016	10001 ~ 10016
Output Coil	0001 ~ 0024	00001 ~ 00024
Input Register	3001 ~ 3002	30001 ~ 30002
Output Register	4001 ~ 4002	40001 ~ 40002
	4001 ~ 4008	40001 ~ 40008

Fig. 3.1 Interface of CPU Module and External Devices

3.4 B2802 OPERATION FLOW

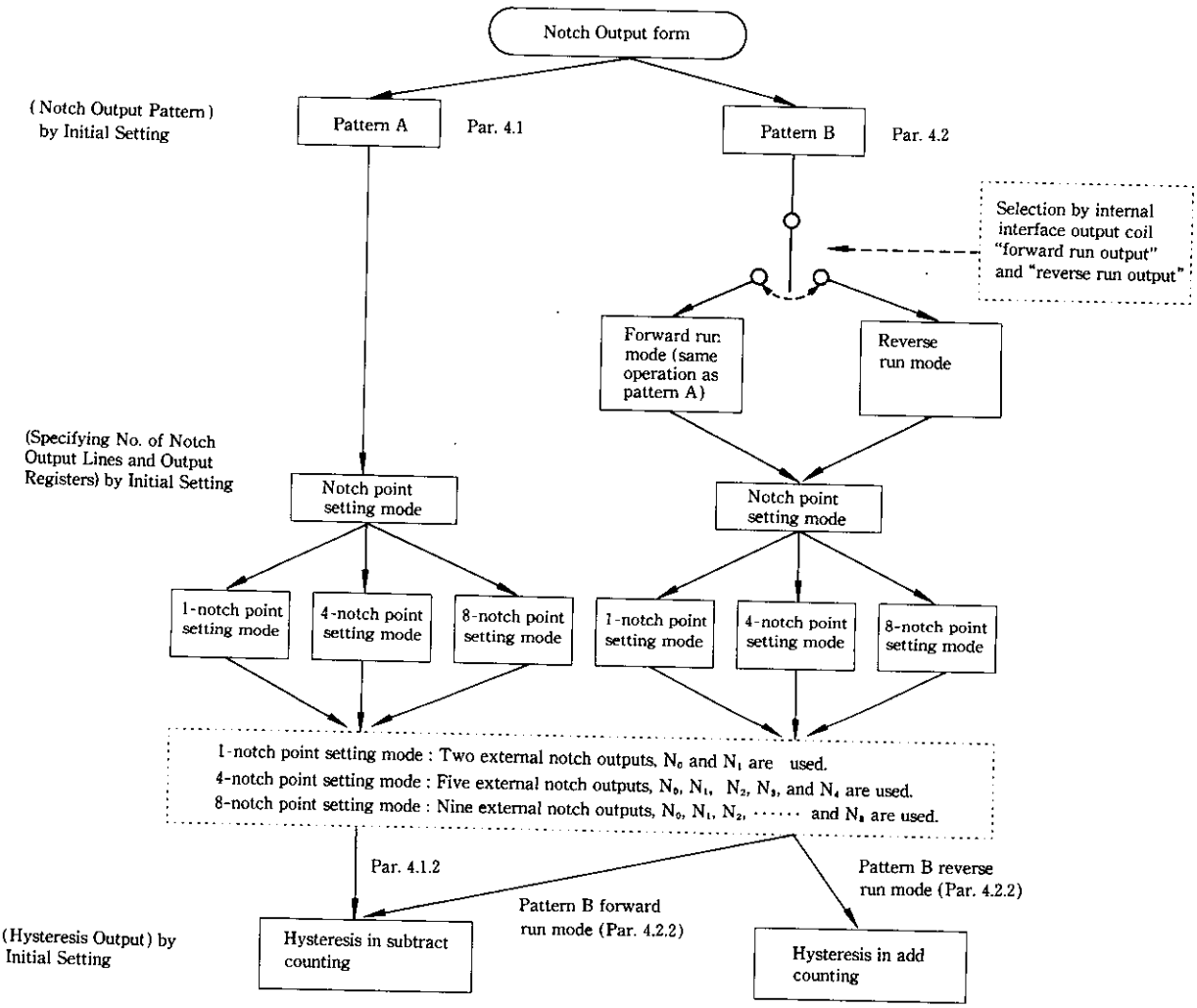
Fig. 3.2 shows B2802 operation outline flow.
(The reference numbers here are given as an example.)



4. COUNTER FUNCTION (NOTCH OUTPUT)

B2802 has 9 external notch outputs (N_0, N_1, $\cdots\cdots$ N_8). When the CPU module presets the notch point set values, B2802 compares the pulse count (current counter reading) with the notch point set value, and outputs notch signals one after another in accordance with the comparison. Notch points are set in three modes: 1-notch point setting, 4-notch point setting and 8-notch point setting. Select among these modes in accordance with the request such as economizing on the number of required notch outputs or output registers, given by the system.

The notch output is in two patterns: A and B. Pattern B is either forward run or reverserun for convenient mixing of the two run directions. The notch output may also be given hysteresis.



4.1 PATTERN A NOTCH OUTPUT

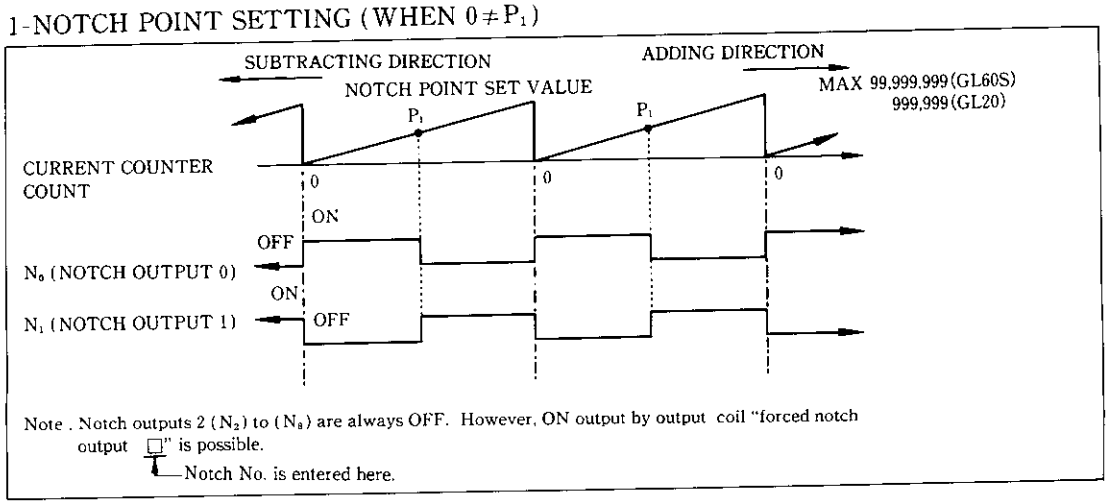
4.1.1 Notch Output (Pattern A)

(1) Basic Form of 1-Notch Output (Pattern A)

(a) 1-Notch point setting mode

Two notches, N_0 (notch output 0) and N_1 (notch output 1), are used. Set the N_1 notch point P_1.

1-NOTCH POINT SETTING (WHEN $0 \neq P_1$)



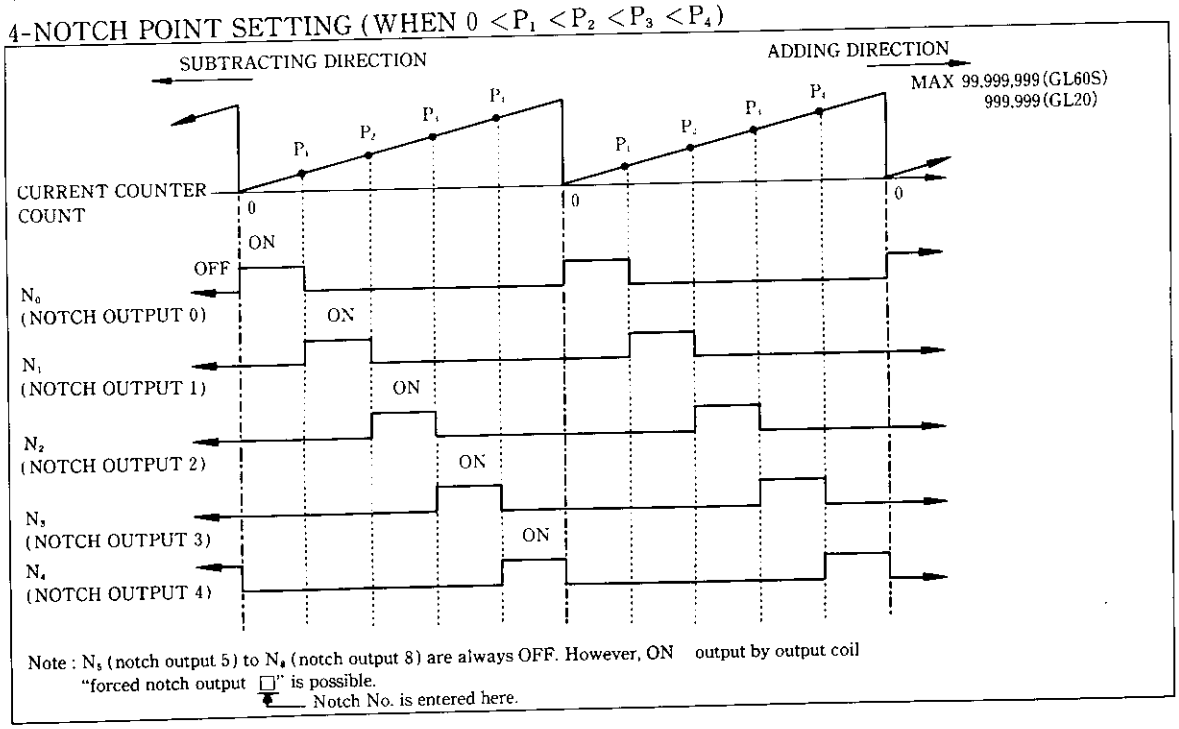
Note . Notch outputs 2 (N_2) to (N_8) are always OFF. However, ON output by output coil "forced notch output □" is possible.
□ ← Notch No. is entered here.

Fig. 4.2 Basic Form (Pattern A) at 1-notch Point Setting

(b) 4-Notch point setting mode

Five notches, N_0 (notch output 0) to N_4 (notch output 4), are used. Set N_1 notch point P_1, N_2 notch point P_2, N_3 notch point P_3, and N_4 notch point P_4.

4-NOTCH POINT SETTING (WHEN $0 < P_1 < P_2 < P_3 < P_4$)



Note : N_5 (notch output 5) to N_8 (notch output 8) are always OFF. However, ON output by output coil "forced notch output □" is possible.
□ ← Notch No. is entered here.

Fig. 4.3 Basic Form (Pattern A) at 4-notch Point Setting

(c) 8-Notch point setting mode

Nine notches, N_0 (notch output 0) to N_8 (notch output 8) are used. Set N_1 notch point P_1, N_2 notch point P_2, N_3 notch point P_3····and N_8 notch point P_8.

8-NOTCH POINT SETTING (WHEN $0<P_1<P_2<P_3<P_4<P_5<P_6<P_7<P_8$)

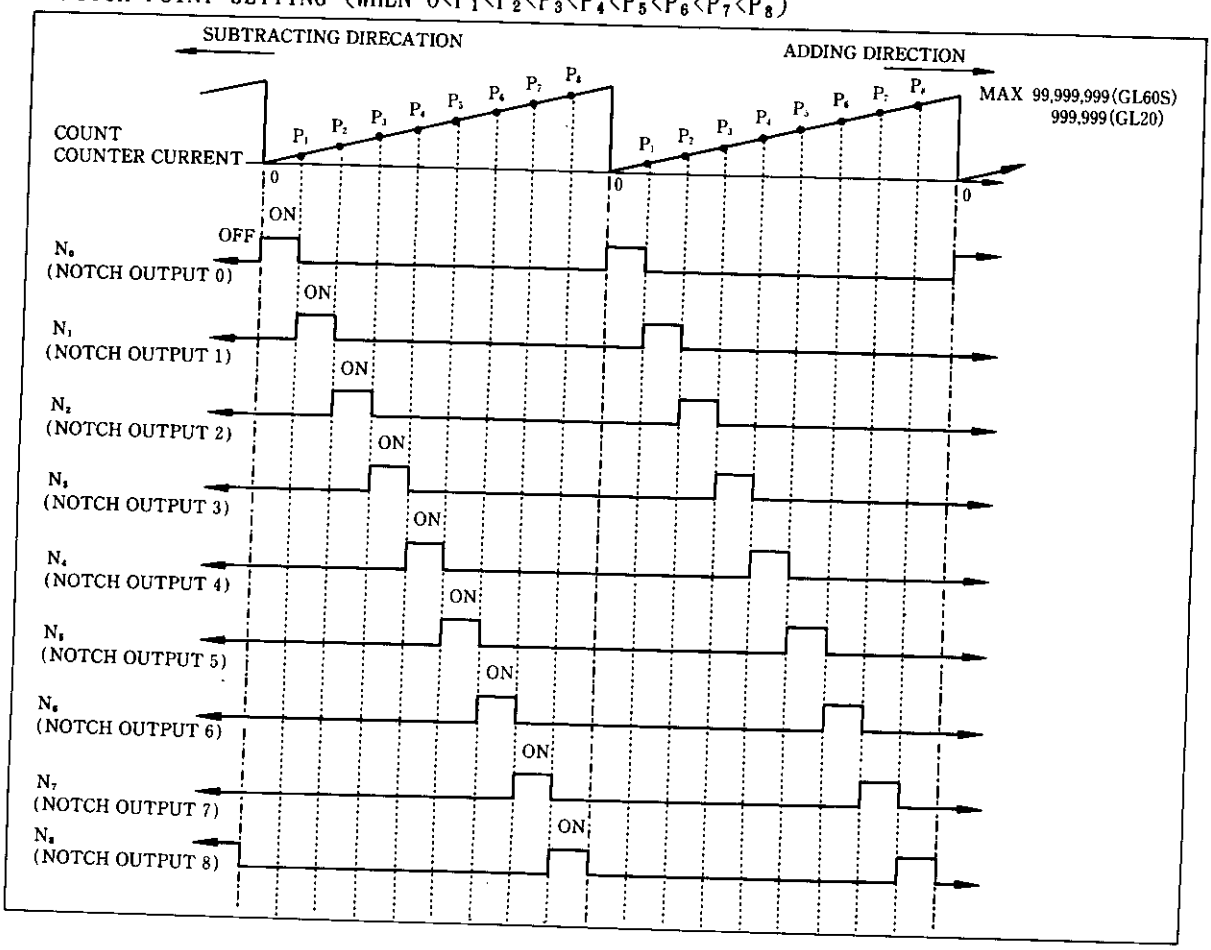


Fig. 4.4 Basic Form at 8-notch Point Setting (Pattern A)

4.1.1 Notch Output (Pattern A) (Cont'd)

(2) Application of Notch Output

(a) The same notch point can be set with the 4-notch point setting and the 8-notch point setting. The notch outputs with the same notch point provide the same ON/OFF operation. Assume N_1 notch point to be P_1, N_2 notch point to be P_2, N_3 notch point to be P_3 and N_4 notch point to be P_4.

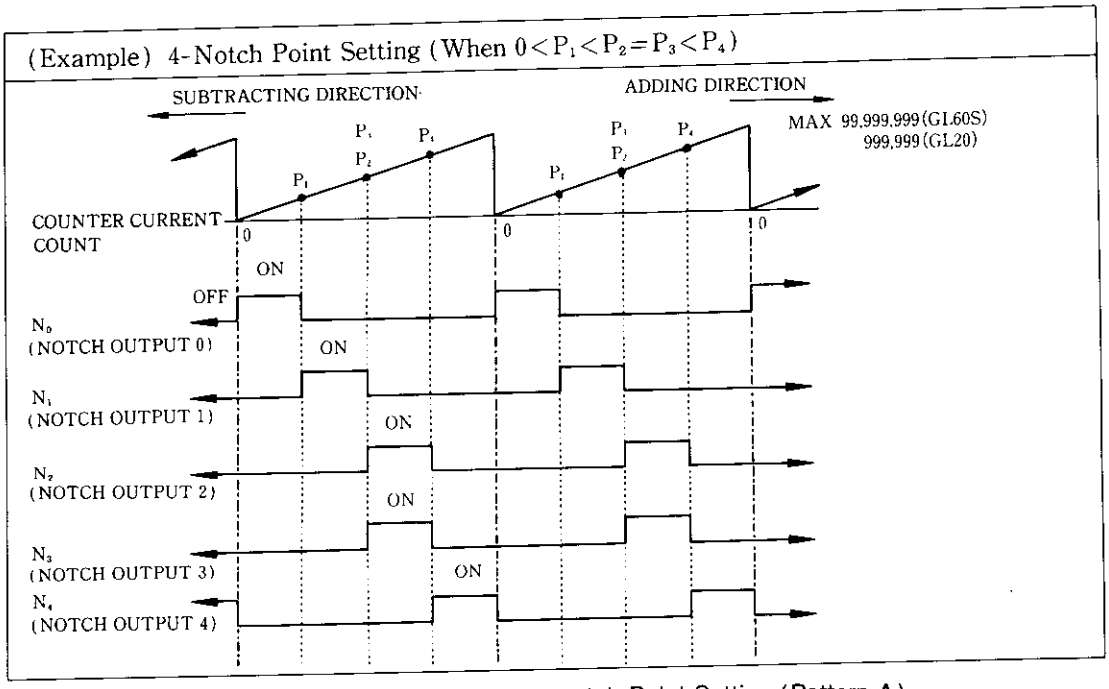


Fig. 4.5 Application 1 at 4-notch Point Setting (Pattern A)

(b) With the 4-notch point setting and the 8-notch point setting, the notch point setting value magnitude combination is free. N_1 notch point is assumed to be P_1, N_2 notch point to be P_2, N_3 notch point to be P_3 and N_4 notch point to be P_4.

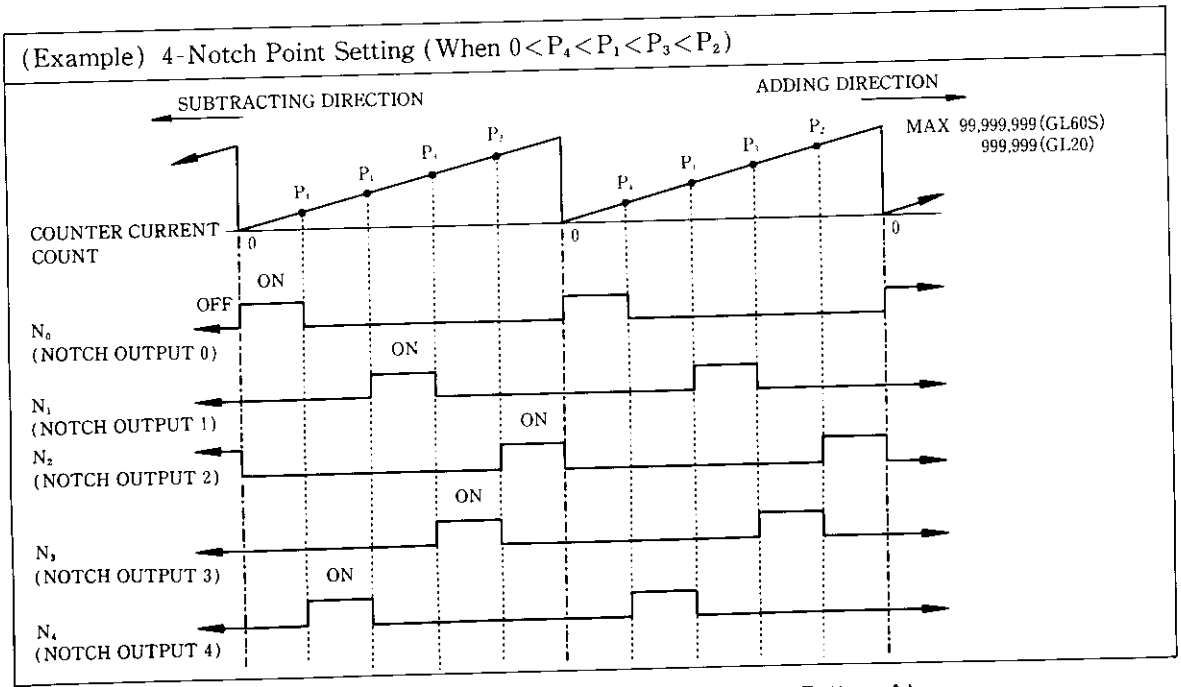


Fig. 4.6 Application 2 at 4-notch Point Setting (Pattern A)

(3) Precautions on Pattern A Notch Output

(a) When the power supply is turned on, modules are reset, and initial setting is made, all the notch point setting values in the module become 0. Until notch points are preset, the output of N_0 (notch output 0) through N_8 (notch output 8) are OFF. However, ON ⟷ OFF output by output coil "forced notch output□" is possible.

(b) When notch point is set for 0, that notch output does not turn ON. Set the unused notch outputs among the 4-notch point setting and the 8-notch point setting to 0. ON ⟷ OFF output by "forced notch output□" is possible.

(c) When the notch point interval including the 0 point is narrow, notch output may be skipped at fast counter counting. Assure at least 5 ms notch point intervals.

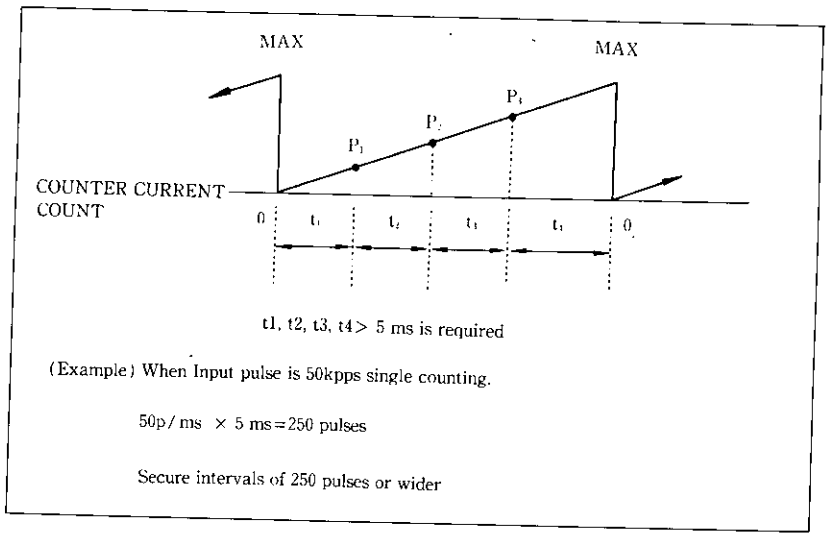


Fig. 4.7 Notch Point Interval Condition

(d) The response time from pulse input to notch output ON-OFF change is 5 msec max.

4.1.2 Hysteresis (Pattern A)

The notch output changeover in the subtracting direction may be given hysteresis. (Operation becomes the same as the pattern B forward run mode.) Set the hysteresis width (0 to 99 pulses) by the initial setting.

(1) Notch Output When Hysteresis Width is Set

(Example) Ni (i : 1, 2, ····, 8) notch point set value is P_i, and the hysteresis width is W (pulses).

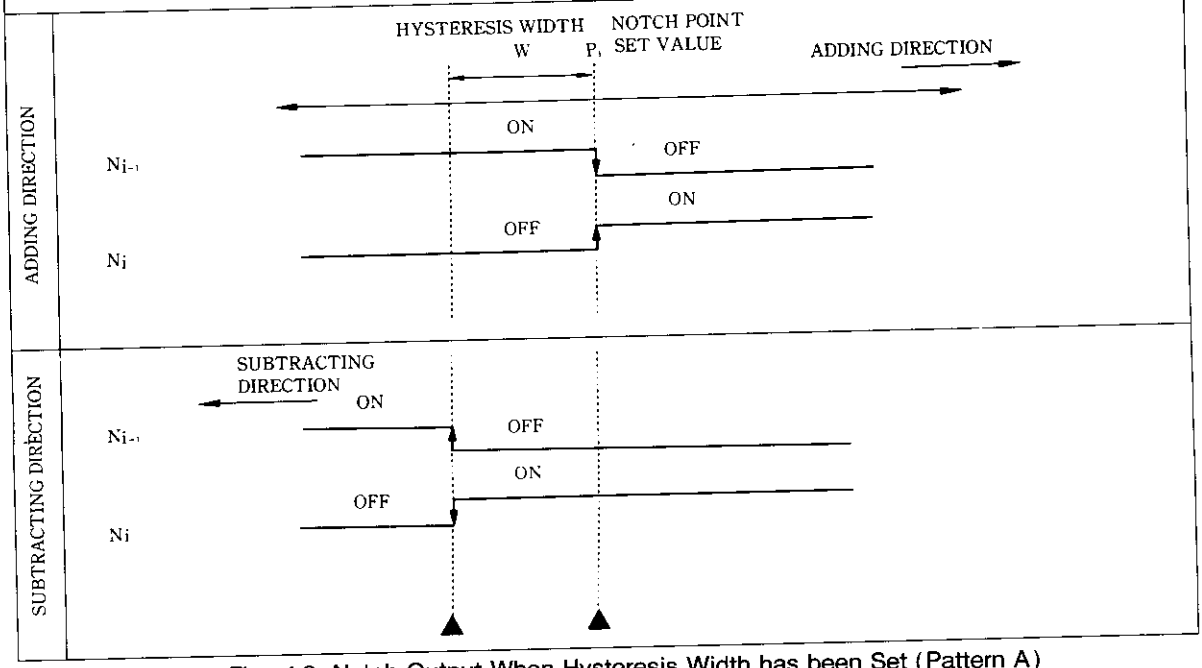


Fig. 4.8 Notch Output When Hysteresis Width has been Set (Pattern A)

(Example) Ni notch point set value = 100, hysteresis width = 50 (pulses) and pulse count single counting are assumed.

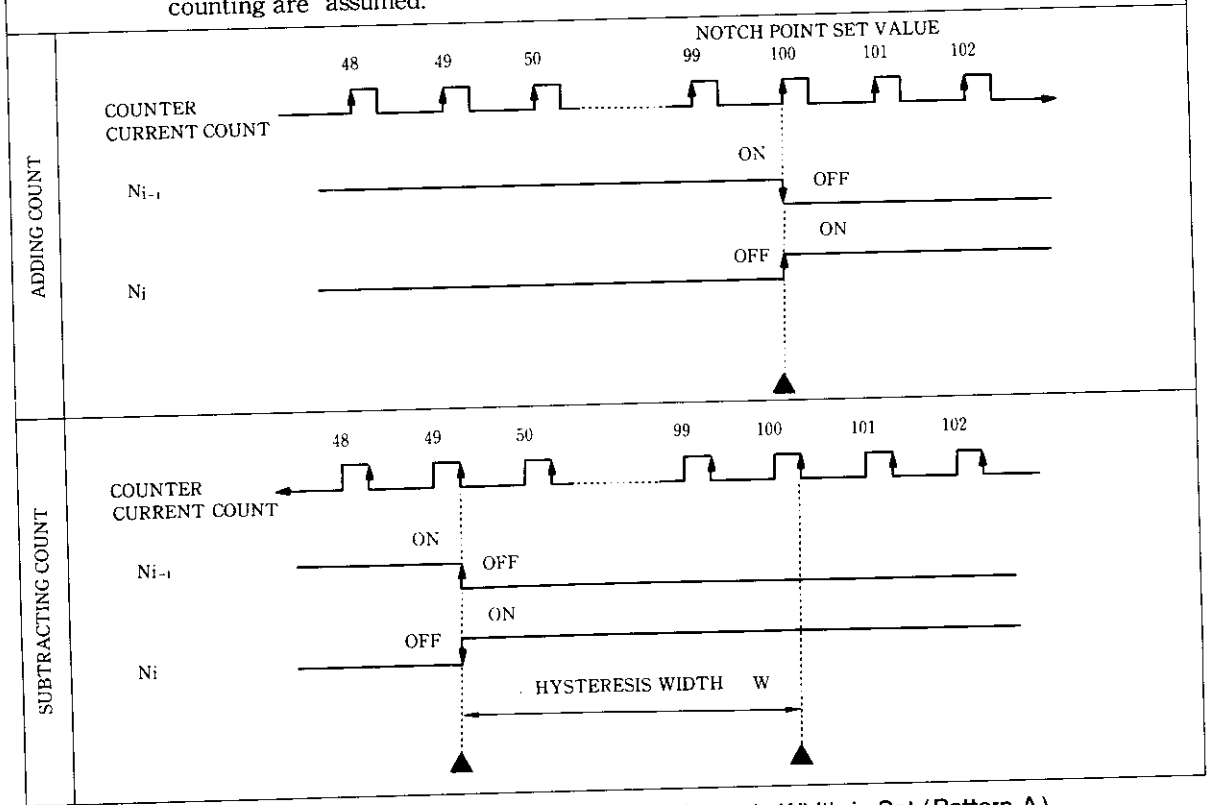


Fig. 4.9 Notch Output Example When Hysteresis Width is Set (Pattern A)

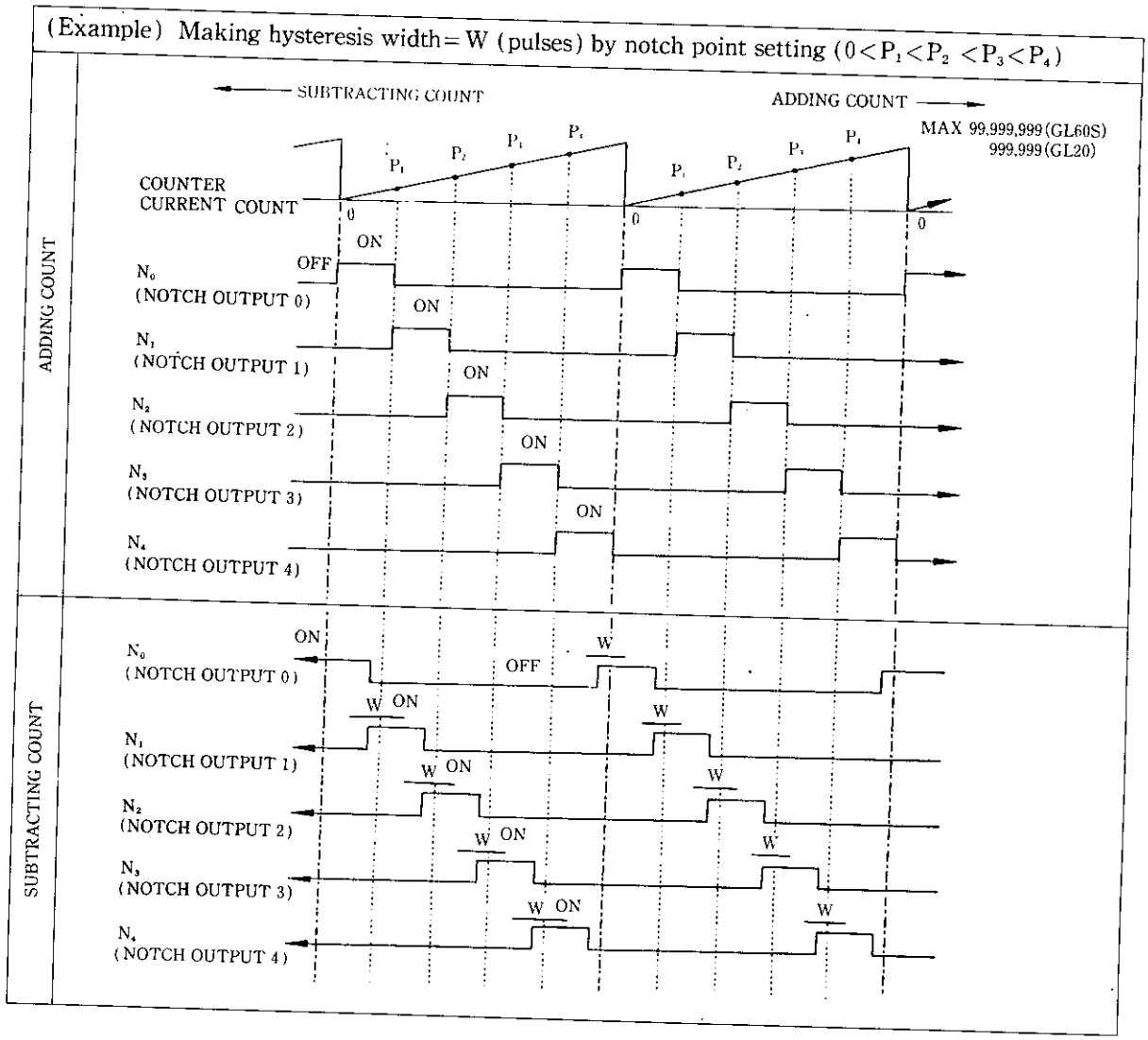


Fig. 4.10 Hysteresis Notch Output at 4-notch Point Setting (Pattern A)

(2) Precautions on Hysteresis (Pattern A)

(a) The hysteresis width setting is common to all the notch output signals. Hysteresis is present also at the MAX ⟷ 0 changeover.

(b) When the hysteresis width is 0 pulse, no hysteresis operation is executed. The notch output changeover point also becomes the same as the adding direction and subtracting direction.

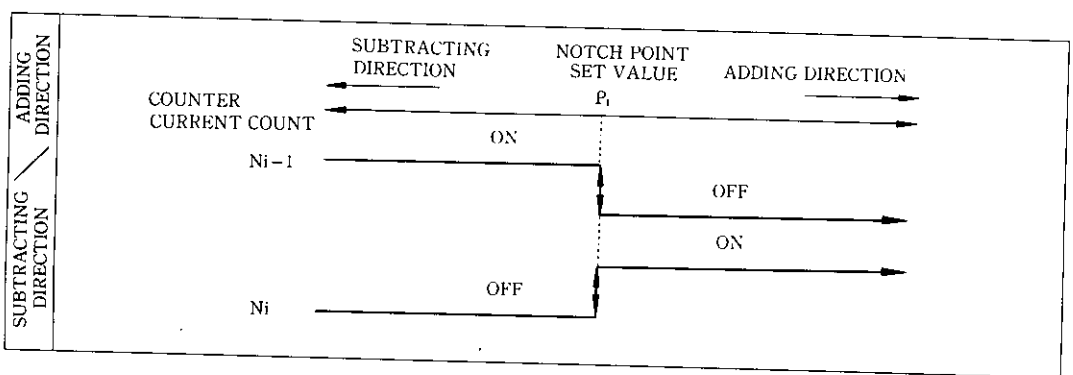


Fig. 4.11 When Hysteresis Width Setting = 0 (Pattern A)

4.1.2 Hysteresis (Pattern A) (Cont'd)

(c) When executing output coil "current count reset", current count preset command", "notch point preset command" or external input "external reset", notch output hysteresis width becomes invalid.

The notch output hysteresis operation is valid only for adding and subtracting the current count by external pulse inputs and add/subtract test pulse inputs.

(d) When the respective notch point setting intervals including the current count = 0 is narrower than the hysteresis width, the notch output becomes ON at the set value in the adding direction, and in the subtracting direction, the resulting output does not turn ON by the hysteresis operation.

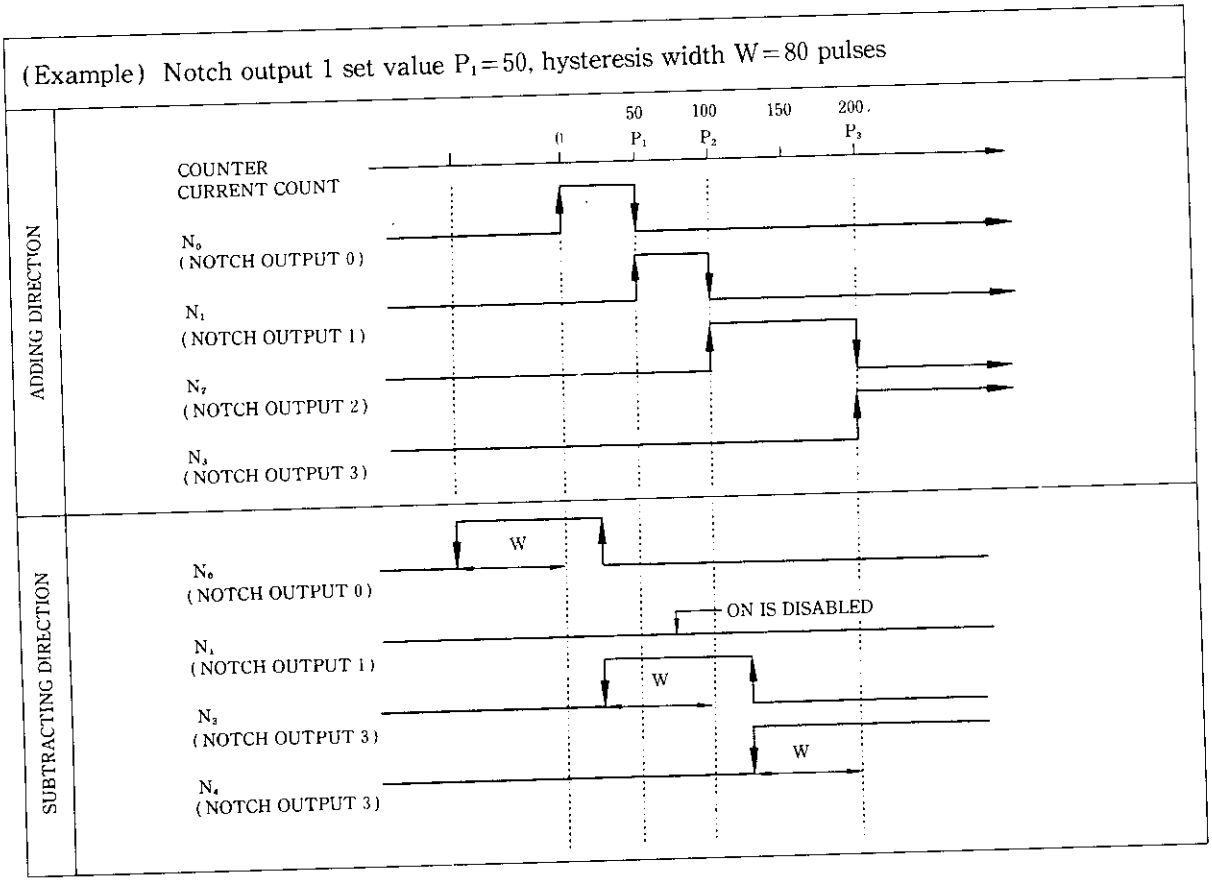


Fig. 4.12 When Hysteresis Width > Notch Point Interval (Pattern A)

4.2 PATTERN B NOTCH OUTPUT

4.2.1 Notch Output (Pattern B)

The pattern B notch output is in two modes; the forward run mode and the reverse run mode. The selection between the two is effected by the ON/OFF combination of the output coil "forward run output" and the "reverse run output". Since the notch output setting is in 3 modes: 1-, 4-and 8-notch point setting, select them (initial setting) to suit to the system. The notch output becomes effective when the output coil "output enable" is ON.

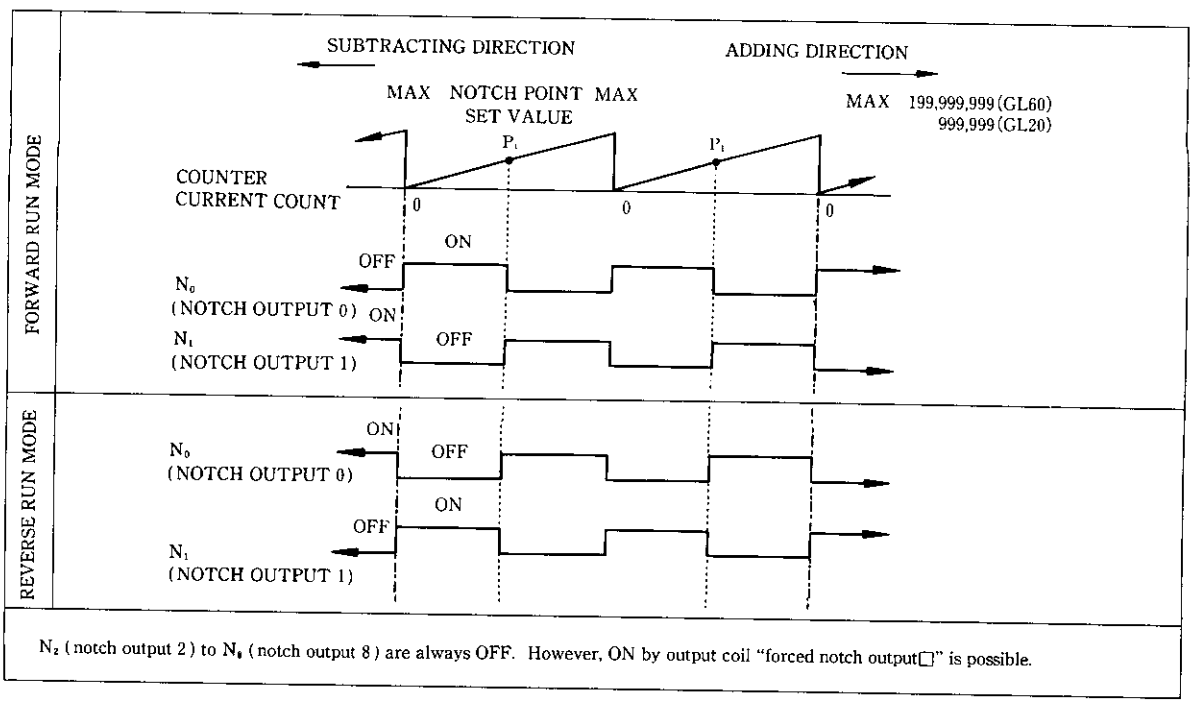
Table 4.1 Forward/Reverse Run Mode Selection

Reference No.	0008+8n	0009+8n	Pattern B	Remarks
Name	Forward Run	Reverse Run		
State	OFF	OFF	Forward run mode	Same as pattern A operation
	ON	OFF	Forward run mode	
	ON	ON	Forward run mode	
	OFF	ON	Reverse run mode	

(1) Notch Output Basic Form (Pattern B)

(a) 1-Notch point setting mode

Two notches, N_0 (notch output 0) and N_1 (notch output 1) are used. Set N_1 notch point P_1.



N_2 (notch output 2) to N_8 (notch output 8) are always OFF. However, ON by output coil "forced notch output□" is possible.

Fig. 4.13 Basic Form at 1-notch Point Setting (Pattern B)

4.2.1 Notch Output (Pattern B) (Cont'd)

(b) 4-Notch point setting mode

Five notches from N_0 (notch output 0)to N_4 (notch output 4) are used. Set the N_1 notch point P_1, N_2 notch point P_2, N_3 notch point P_3, and N_4 notch point P_4.

4-NOTCH POINT SETTING (WHEN $0< P_1<P_2<P_3<P_4$)

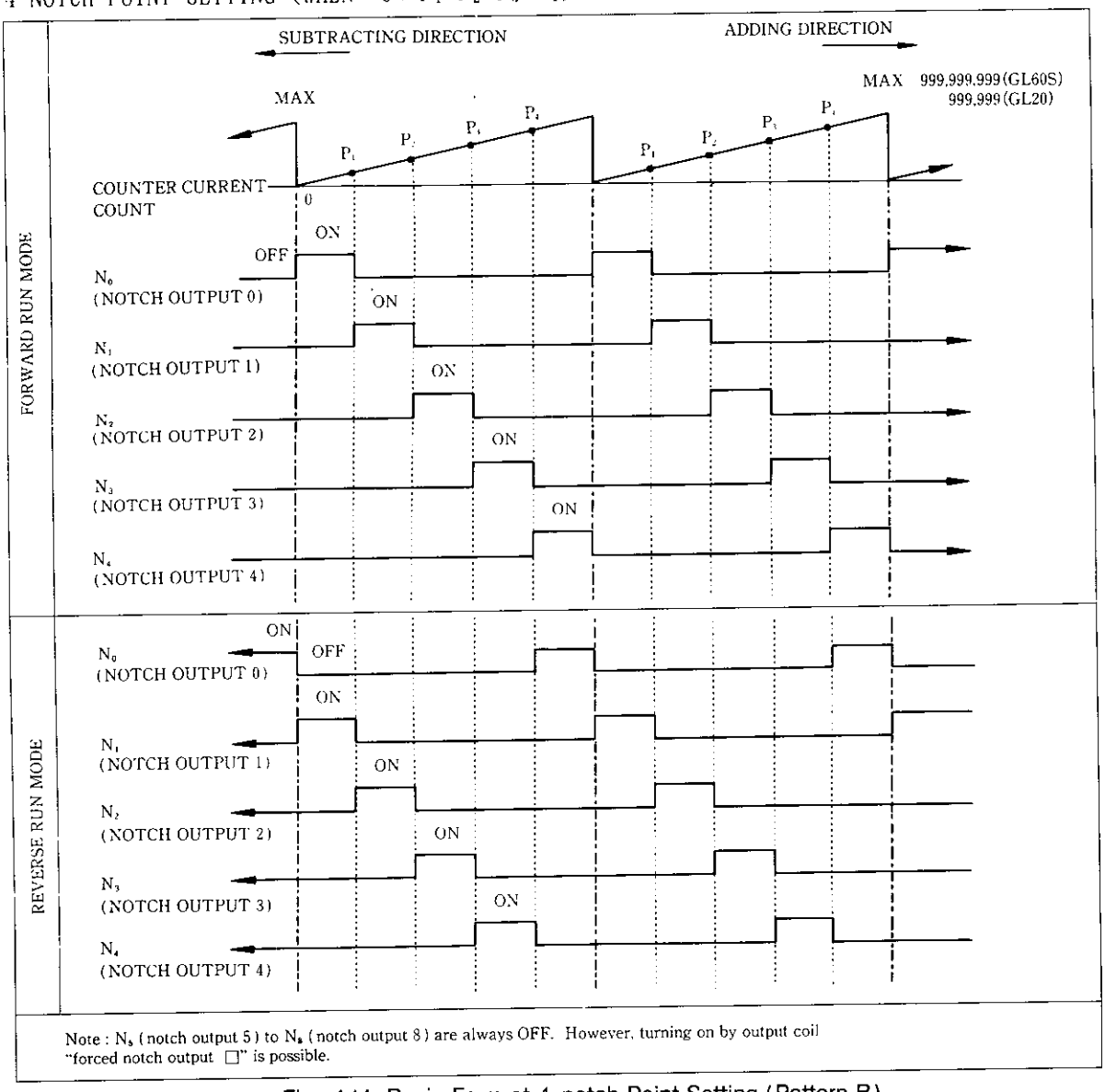


Fig. 4.14 Basic Form at 4-notch Point Setting (Pattern B)

(c) 8-Notch point setting mode

Nine notches, N_0 (notch output 0) to N_8 (notch output 8) are used. Set the N_1 notch point P_1, N_2 notch point P_2, N_3 notch point P_3, N_4 notch point P_4, N_5 notch point P_5, N_6 notch point P_6, N_7 notch point P_7, and N_8 notch point P_8.

8-NOTCH POINT SETTING
(WHEN $0<P_1<P_2<P_3<P_4<P_5<P_6<P_7<P_8$)

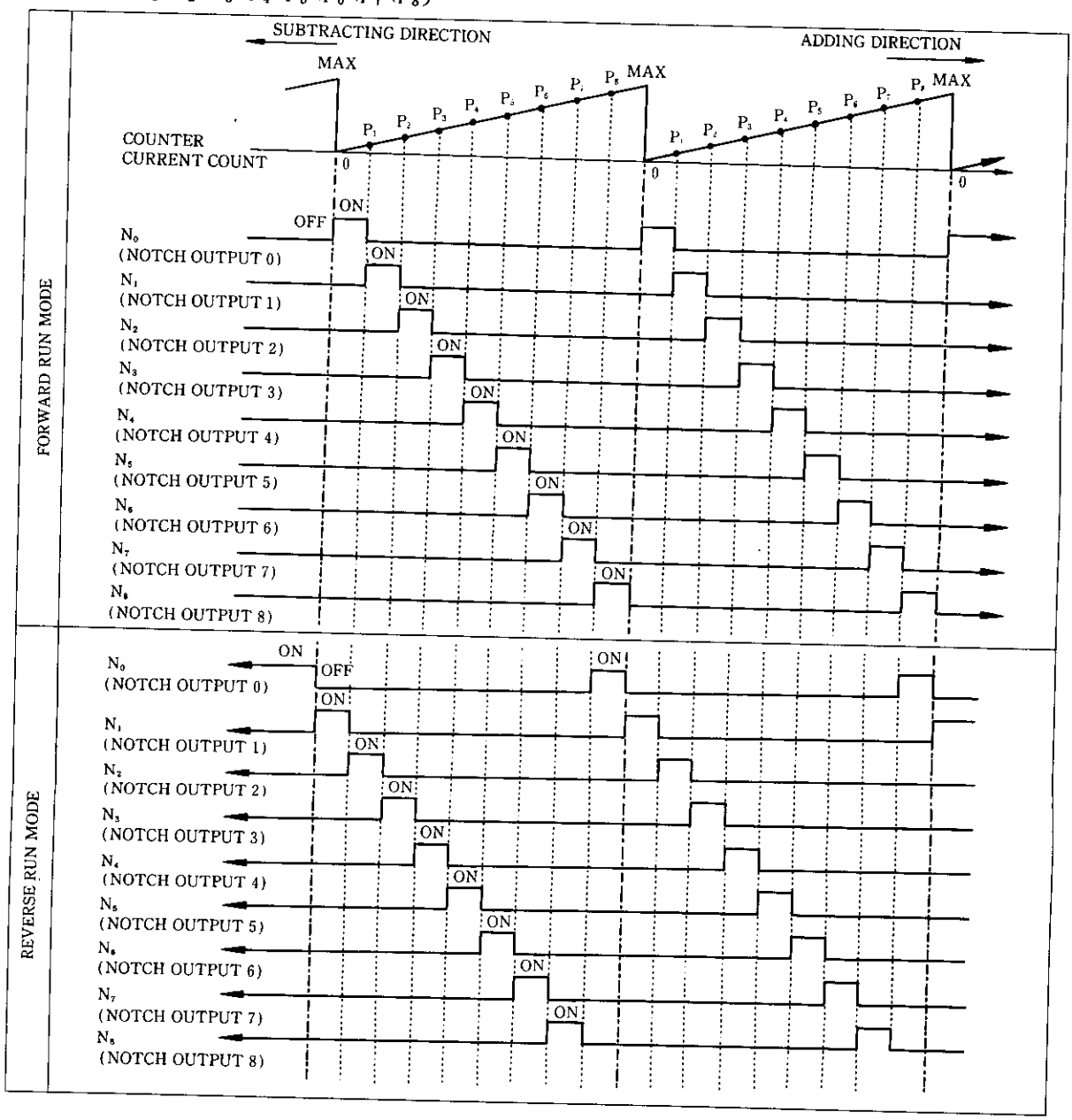


Fig. 4.15 Basic Form at 8-notch Point Setting (Pattern B)

4.2.1 Notch Output (Pattern B) (Cont'd)

(2) Notch Output Application (Pattern B)

(a) With the 4-notch setting and the 8-notch setting, the same notch point can be set. The notch output with the same notch point executes the same ON ⟷ OFF operation. Set the N_1 notch point P_1, N_2 notch point P_2, N_3 notch point P_3 and N_4 notch point P_4.

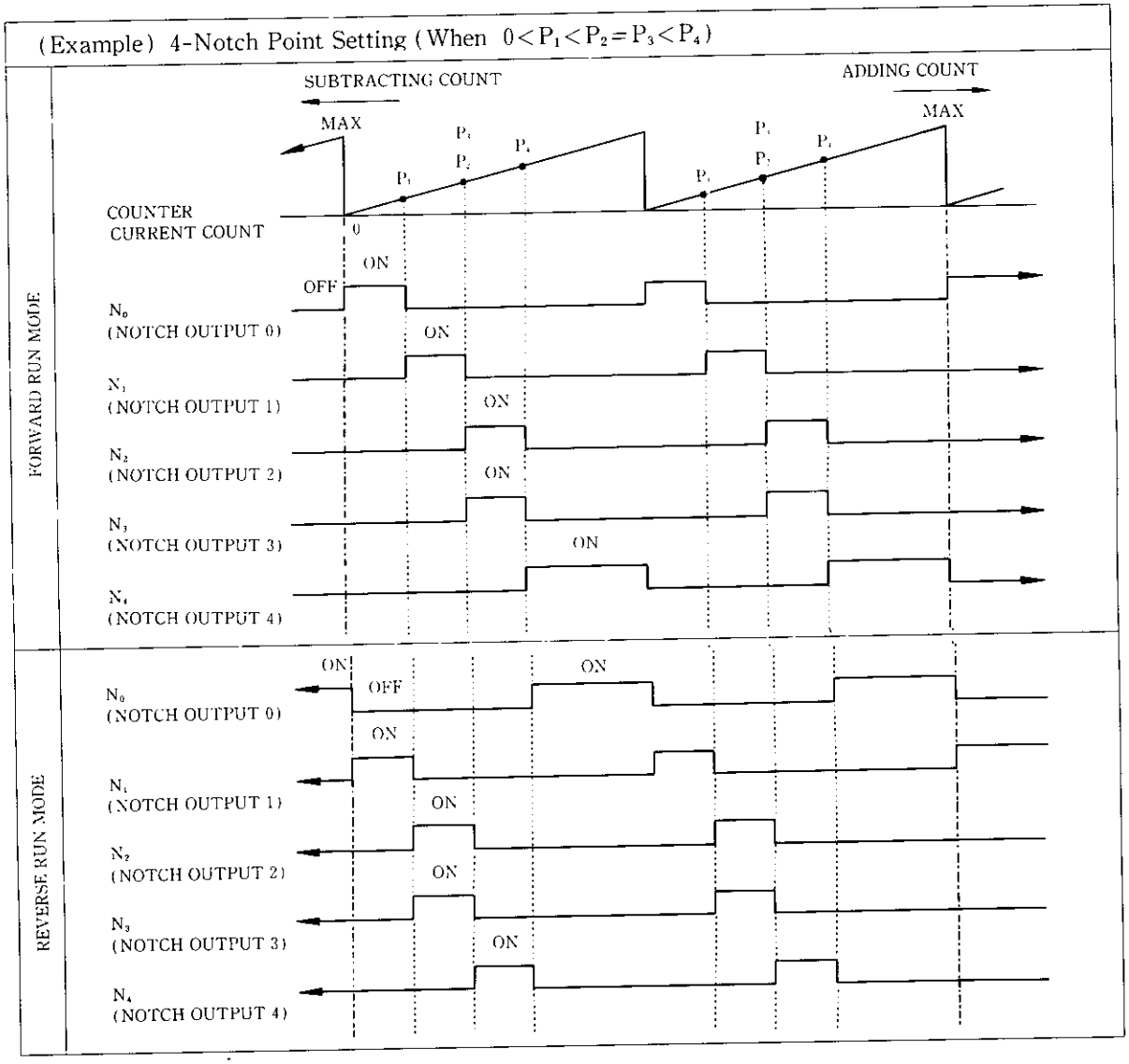


Fig. 4.16 Application 1 at 4-notch Point Setting (Pattern B)

(b) With the 4-notch setting and 8-notch setting, the magnitude relationship among the notch point settings can be combined freely. Set the N_1 notch point P_1, N_2 notch point P_2, N_3 notch point P_3, and N_4 notch point P_4.

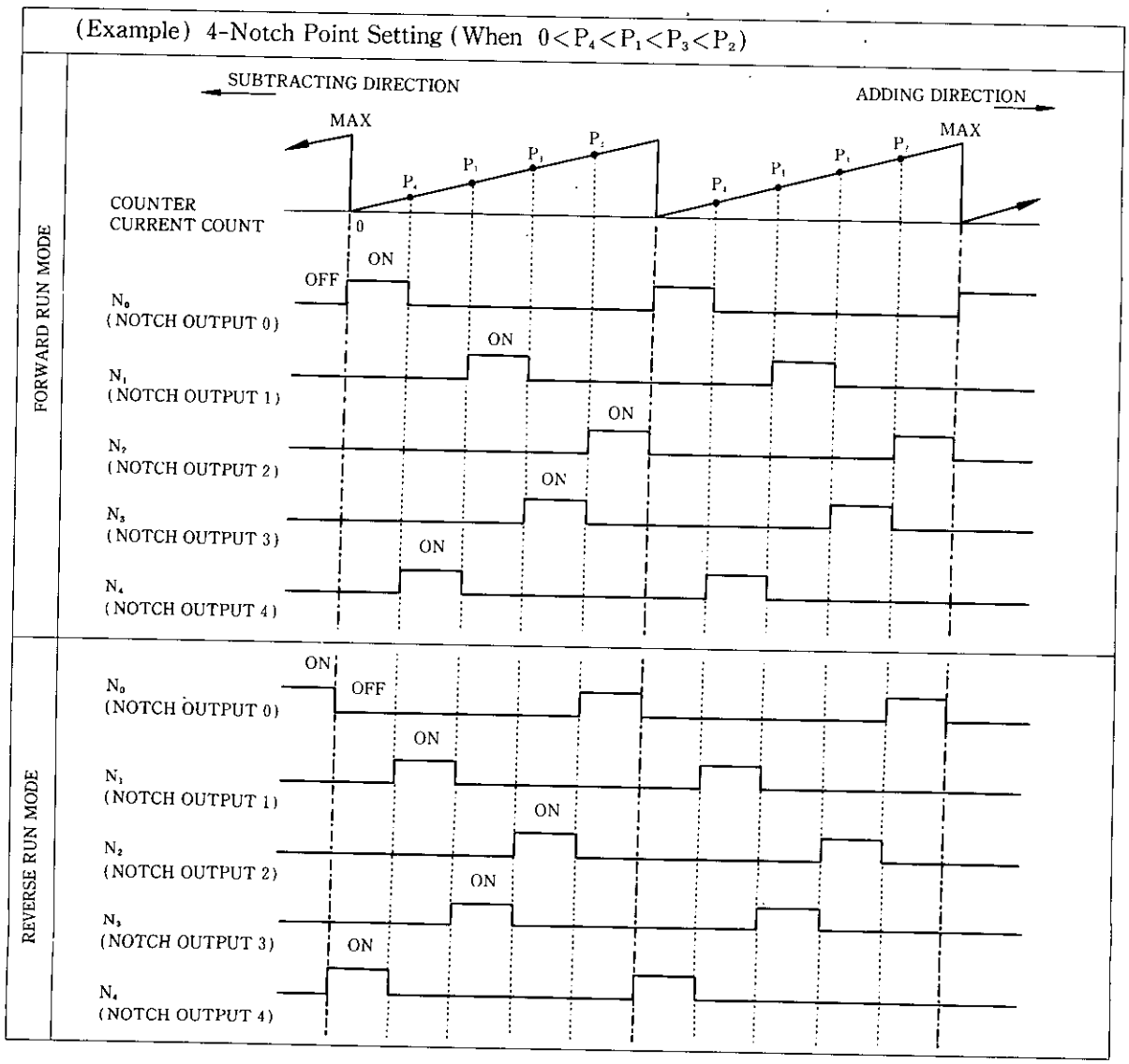


Fig. 4.17 Application 2 at 4-notch Point Setting (Pattern B)

4.2.1 Notch Output (Pattern B) (Cont'd)

(3) Precautions on Pattern B Notch Output

(a) After specifying pattern B in the initial setting, the notch point set value is 0 until the notch point is preset. The output from N_0 (notch output 0) to N_8 (notch output 8) is OFF. However, the ON ⟷ OFF output by the output coil "forced notch output□" is possible.

(b) When the notch point set value is 0, its notch output cannot be turned on. Set the unused notch outputs among the 4-notch point setting and 8-notch point setting to 0. Still, ON ⟷ OFF output by "forced notch output□" is possible.

(c) When the notch point intervals including the 0 point are narrow, notch output may be skipped at high speed counting. Secure at least 5ms for the notch intervals.

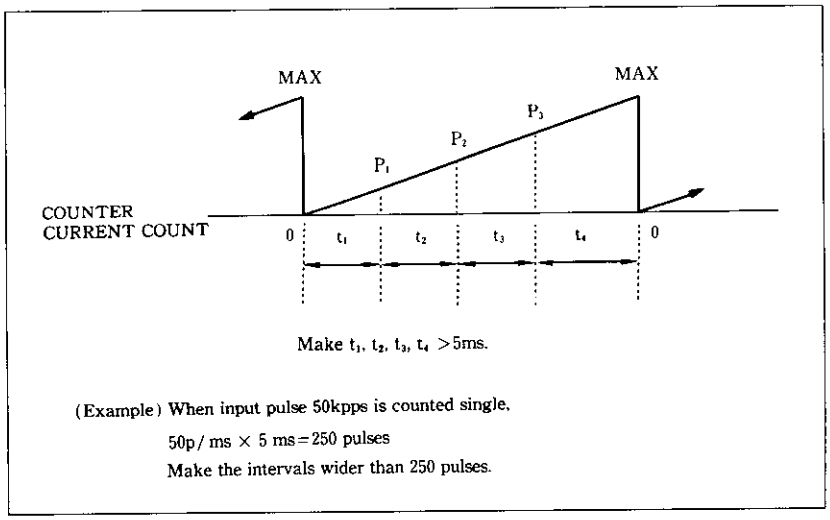


Fig. 4.18 Notch Point Interval Condidtion

(d) The response time from pulse input to external notch output ON ⟷ OFF change is less then 5ms.

4.2.2 Hysteresis (Pattern B)

The notch output changeover point differs between the forward run mode and the reverse run mode. Set the hysteresis width (0 to 99 pulses) common to all the notch output signals by the initial setting.

(1) Notch Output at Hysteresis Width Setting

Set the Ni notch point to P_i, and the hysteresis width to W (pulses).
[i=1, 2, ····, 8]

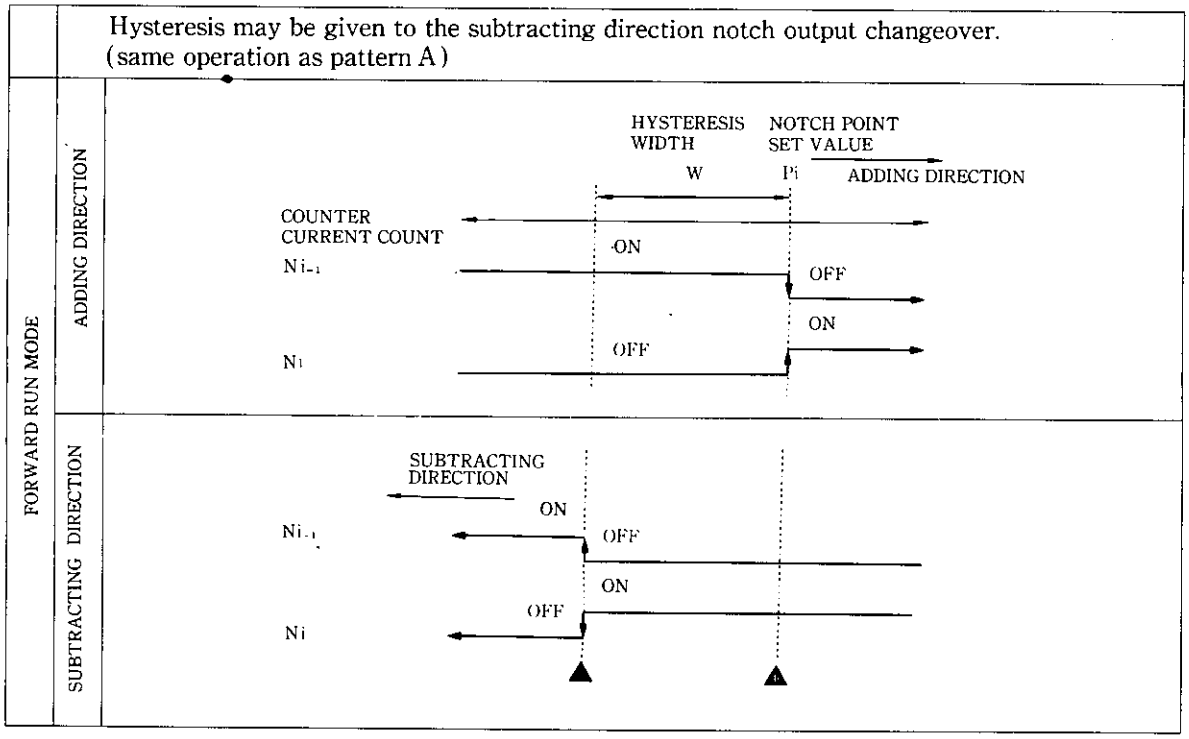


Fig. 4.19 Hysteresis Operation at Forward Run Mode (Pattern B)

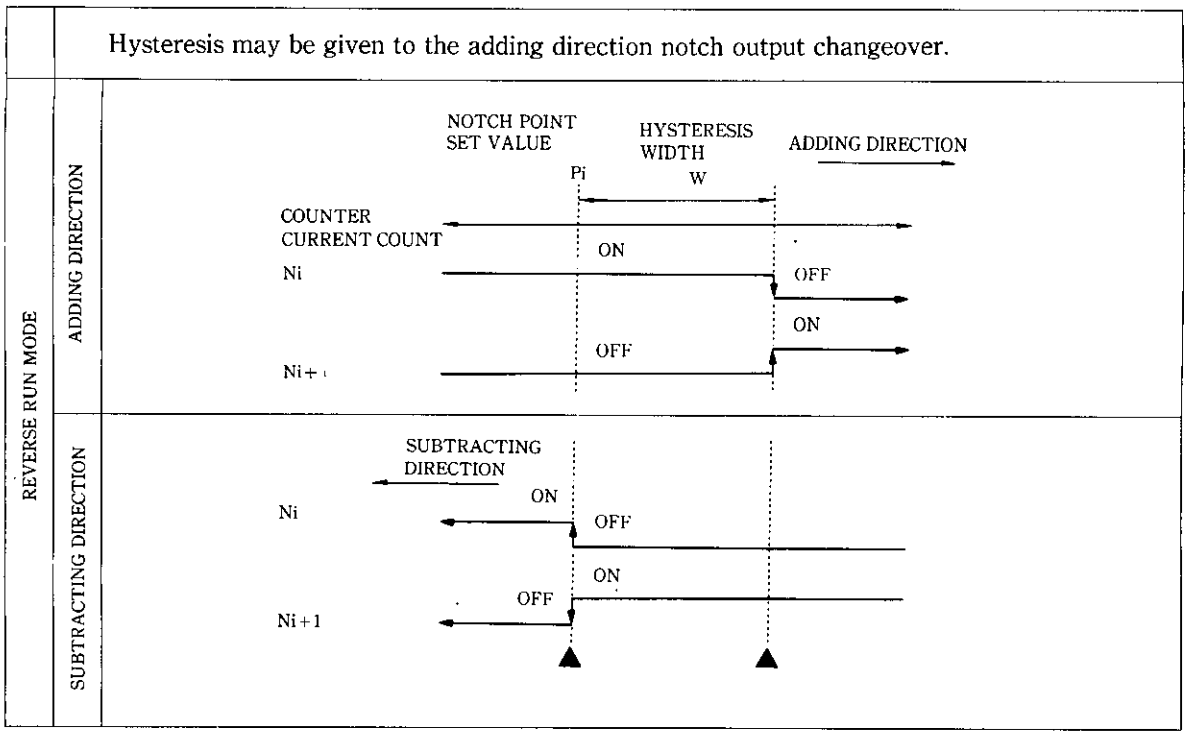


Fig. 4.20 Hysteresis Operation at Reverse Run Mode (Pattern B)

4.2.2 Hysteresis (Pattern B) (Cont'd)

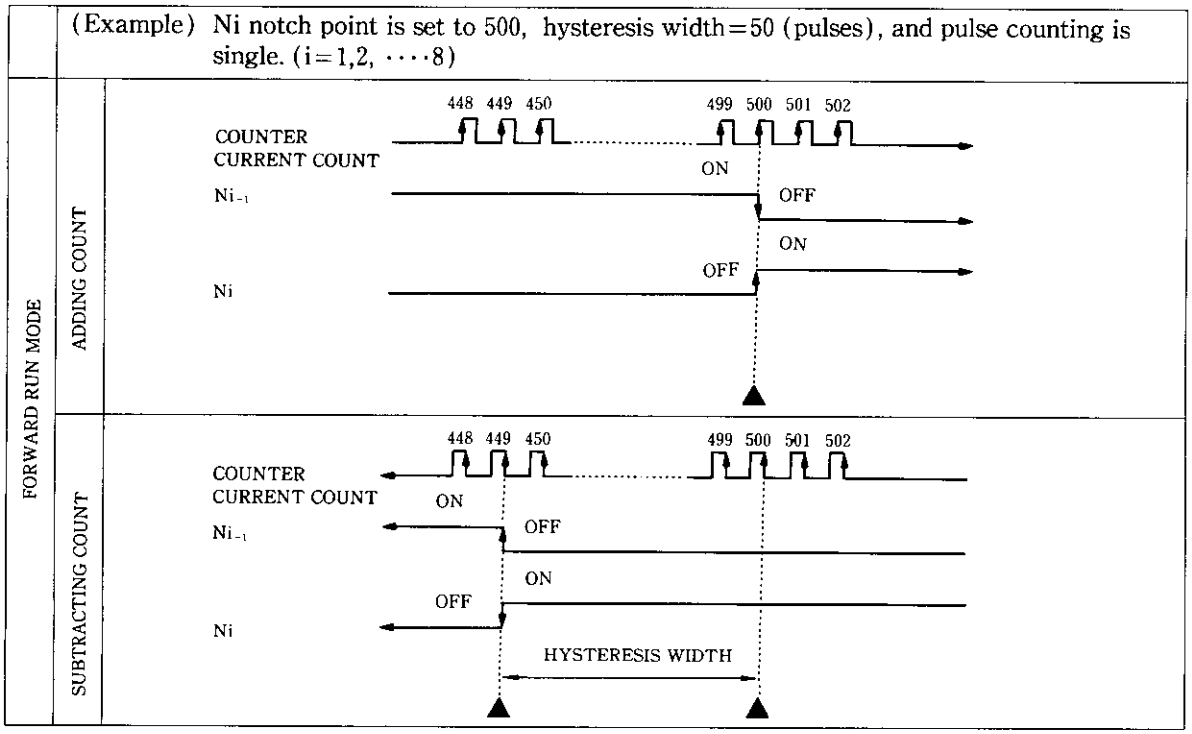


Fig. 4.21 Hysteresis Operation at Forward Run Mode (Pattern B)

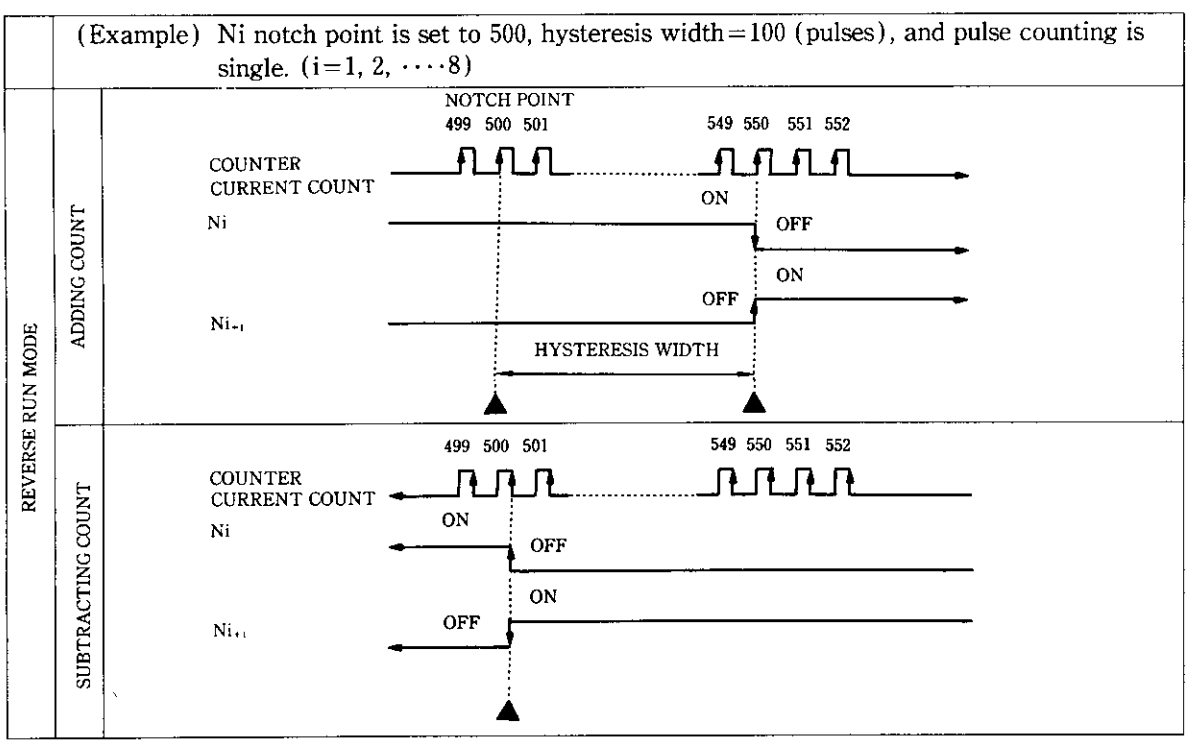


Fig. 4.22 Hysteresis Operation at Reverse Run Mode (Pattern B)

(2) Precautions on Hysteresis (Pattern B)

(a) The hysteresis width becomes the same for all notch output changeovers.

(b) When the hysteresis width is 0 pulse, there is no hysteresis operation. The notch output changeover becomes the same in both the adding and subtracting directions.

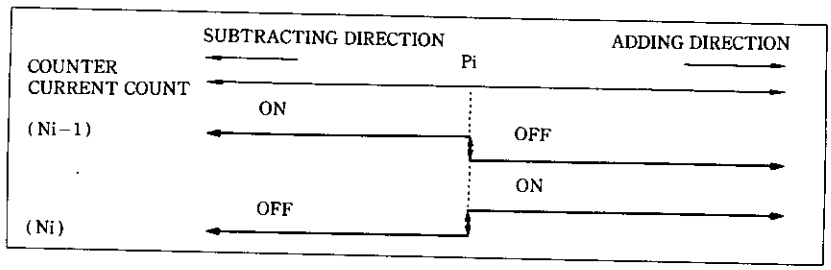


Fig. 4.23 When Hysteresis Width Setting = 0 (Pattern B)

(c) When executing "current value reset", "current value preset command", "Notch point preset command" for the output coil, or "external reset" for external input, the notch output hysteresis width is invalid. The same applies when changing over between forward and reverse.

The notch output hysteresis operation is valid only when executing the current count addition or subtraction by external pulse input, or add test or subtract test pulse input.

(d) When the notch point setting intervals including the current count 0 point are narrower than the hysteresis width, the notch output is turned on at the set value in the adding direction, and in the subtracting direction, some notch outputs are not turned on due to the hysteresis operation, and vice versa. (Fig. 4.24)

4.2.2 Hysteresis (Pattern B) (Cont'd)

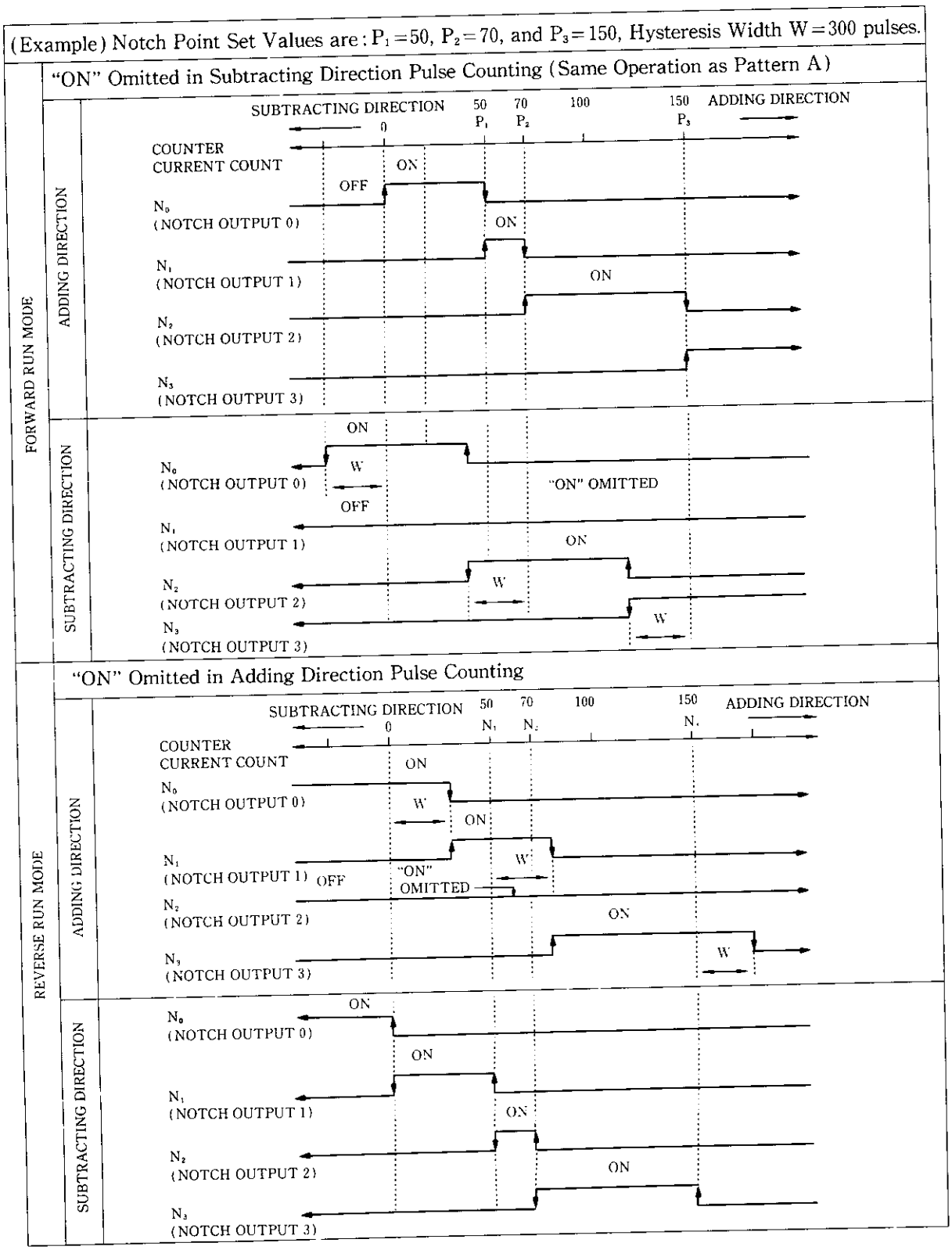


Fig. 4.24 When Hysteresis Width > Notch Point Interval (Pattern B)

5. INTERNAL INTERFACE

5.1 CPU MODULE I/O ALLOCATION

The output coil, input relay, output register and the input register are allocated to the internal interfaces between the CPU module and B2802. The number of CPU module I/O allocations is shown in Table 5.1. When allocating the output register and input register, specify BINARY.

Table 5.1 Number of CPU Module I/O Allocation Points

I/O Allocation / Name	Points/Registers	Signal Flow	
		CPU Module	B2802
Output Coil	24 (16 possible)	→	
Input Relay	16 (8 possible)	←	
Output Register	2 or 8	→	
Input Register	2	←	

5.2 OUTKPUT COIL (CONTROL SIGNAL) FOR CPU MODULE TO B2802

(1) Output Coil List

There are 24 output coils (16 are possible), activating as control signals from the CPU module to B2802. Table 5.2 is the output coil list.

Table 5.2 Output Coil List

GL20	GL60S	Signal Name
0001 + 8n	00001 + 8n	Module reset
0002 + 8n	00002 + 8n	Initial setting
0003 + 8n	00003 + 8n	Current count reset
0004 + 8n	00004 + 8n	Countable
0005 + 8n	00005 + 8n	Output enable
0006 + 8n	00006 + 8n	Current count preset command
0007 + 8n	00007 + 8n	Notch point preset command
0008 + 8n	00008 + 8n	Forward run output
0009 + 8n	00009 + 8n	Reverse run output
0010 + 8n	00010 + 8n	Forced notch output 0
0011 + 8n	00011 + 8n	Forced notch output 1
0012 + 8n	00012 + 8n	Forced notch output 2
0013 + 8n	00013 + 8n	Forced notch output 3
0014 + 8n	00014 + 8n	Forced notch output 4
0015 + 8n	00015 + 8n	Forced notch output 5
0016 + 8n	00016 + 8n	Forced notch output 6
0017 + 8n	00017 + 8n	Forced notch output 7
0018 + 8n	00018 + 8n	Forced notch output 8
0019 + 8n	00019 + 8n	Monitor 0
0020 + 8n	00020 + 8n	Monitor 1
0021 + 8n	00021 + 8n	Monitor 2
0022 + 8n	00022 + 8n	Monitor 3
0023 + 8n	00023 + 8n	Reserved for future use
0024 + 8n	00024 + 8n	Reserved for future use

When allocating 16 points, these signals are treated as OFF in the module.

n=0, 1, 2····

Reference Nos. at output coil allocation

(2) Contents of Output Coils

The 24 output coils activate as the control signals shown in Table 5.3. B2802 checks the coil ON/OFF status in accordance with Table 5.4 Output Coil Condition List. Commands not conforming to these conditions are treated as errors. For initial setting, approximately 0.5s is required. Each setting must be performed after more than 0.5s from the module reset.

Table 5.3 Output Coil Signal Names and Contents

Reference No.		Signal Name	Contents
GL20	GL60S		
0001 + 8n	00001 + 8n	Module reset	Module reset command When B2802 receives MODULE RESET, it initializes the internal RAM and external I/O signals. For the initial setting, defaults are set. (See Par. 5.4.1) It becomes valid at OFF to ON.
0002 + 8n	00002 + 8n	Initial setting	B2802 initial setting command (Initial values are set in the output register in advance.) Sets counter function of the module. When the initial setting command is given, the current count, current count preset value, and notch point preset value are cleared, and must be reset. Becomes valid at OFF to ON. Setting is possible while "count enable" coil is OFF. (External "count enable" is irrelevant)
0003 + 8n	00003 + 8n	Current count reset	While "current count reset" is ON, the current count remains 0, and the pulse counting is off. Becomes effective at ON. It is in OR with ON of external reset input signal RST.
0004 + 8n	00004 + 8n	Count enable	When "count enable" is ON, and the external count enable input signal ENB is ON, counter can count pulses. Becomes effective at ON.
0005 + 8n	00005 + 8n	Output enable	While "output enable" is ON, N_0 to N_8(notch outputs 0 - 8), the forward run output and reverse run output can be ON externally. At OFF, all the output signals are turned OFF. Becomes effective
0006 + 8n	00006 + 8n	Current count preset command	Current count preset command (current count is set in the output register in advance) It presets the output register value to the current count. Becomes effective at OFF to ON.
0007 + 8n	00007 + 8n	Notch point preset command	Notch point set value preset command (Notch point set value is set in the output register in advance) Two or eight output registers may be used. Becomes effective at OFF to ON. Be aware that the preset sequence varies with the 1-notch point setting mode, 4-notch point setting mode and 8-notch point setting mode. (See Par. 5.4.2)

5.2 OUTPUT COIL (CONTROL SIGNAL) FOR CPU MODULE TO B2802 (Cont'd)

Table 5.3 Output Coil Signal Names and Contents (Cont'd)

<table>
<tr><th colspan="2">Reference No.</th><th rowspan="2">Signal Name</th><th rowspan="2">Contents</th></tr>
<tr><th>GL20</th><th>GL60S</th></tr>
<tr><td>0008 + 8n</td><td>00008 + 8n</td><td>Forward run output</td><td rowspan="2">The ON/OFF status of the "forward run" and "reverse run" coils becomes the external output "forward run output" and "reverse run output", directly. Output is enabled when "output enable" coil is ON. In the notch output pattern B, it is also used for switching over between "forward run mode" and "reverse run mode". In this case, the ON/OFF status of "output enable" coil becomes irrelevant.</td></tr>
<tr><td>0009 + 8n</td><td>00009 + 8n</td><td>Reverse run output</td></tr>
<tr><td>0010 + 8n</td><td>00010 + 8n</td><td>Forced notch output 0</td><td rowspan="9">When the "forced notch output □" coil is turned on, the "external notch output □" is turned on. However, when any of the forced notch outputs is turned on, the regular notch output is turned off. When all the forced notch output coils are turned off, the regular notch output state is restored.
Forced notch output 0 ⋯▸ corresponds to N_0 (notch output 0)
⟆ ⟆
Forced notch output 8 ⋯▸ corresponds to N_8 (notch output 8)
Two or more ON outputs are possible.
When "output enable" is on, external output is enabled.</td></tr>
<tr><td>0011 + 8n</td><td>00011 + 8n</td><td>Forced notch output 1</td></tr>
<tr><td>0012 + 8n</td><td>00012 + 8n</td><td>Forced notch output 2</td></tr>
<tr><td>0013 + 8n</td><td>00013 + 8n</td><td>Forced notch output 3</td></tr>
<tr><td>0014 + 8n</td><td>00014 + 8n</td><td>Forced notch output 4</td></tr>
<tr><td>0015 + 8n</td><td>00015 + 8n</td><td>Forced notch output 5</td></tr>
<tr><td>0016 + 8n</td><td>00016 + 8n</td><td>Forced notch output 6</td></tr>
<tr><td>0017 + 8n</td><td>00017 + 8n</td><td>Forced notch output 7</td></tr>
<tr><td>0018 + 8n</td><td>00018 + 8n</td><td>Forced notch output 8</td></tr>
<tr><td>0019 + 8n</td><td>00019 + 8n</td><td>Monitor 0</td><td rowspan="4">The following contents may be monitored in the input register by various combinations of monitor coil ON/OFF.
<table><tr><th>Monitor 0</th><th>Monitor 1</th><th>Monitor 2</th><th>Monitor 3</th><th>Contents</th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>Current count</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>N_1 notch point set value</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>N_2 notch point set value</td></tr><tr><td>1</td><td>1</td><td>0</td><td>0</td><td>N_3 notch point set value</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>N_4 notch point set value</td></tr><tr><td>1</td><td>0</td><td>1</td><td>0</td><td>N_5 notch point set value</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>N_6 notch point set value</td></tr><tr><td>1</td><td>1</td><td>1</td><td>0</td><td>N_7 notch point set value</td></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>N_8 notch point set value</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1</td><td>Initial set value</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>Current count preset value</td></tr></table>1 : ON, 0 : OFF
Combinations other than the above bring the counter to the current count.</td></tr>
<tr><td>0020 + 8n</td><td>00020 + 8n</td><td>Monitor 1</td></tr>
<tr><td>0021 + 8n</td><td>00021 + 8n</td><td>Monitor 2</td></tr>
<tr><td>0022 + 8n</td><td>00022 + 8n</td><td>Monitor 3</td></tr>
</table>

(3) Output Coil Condition List

Table 5.4 shows the output coil condition list. Commands not satisfying the output coil ON/OFF conditions become errors.

Table 5.4 Output Coil Condition List

Output Coil Signal Name / Module Operation	Module Reset	Initial Setting	Current Count Reset	Count Enable	Output Enable	Current Count Preset Command	Notch Point Preset Command	Forward/ Reverse Run	Forced Notch 0 to 8	Monitor 0 to 3	Remark
Module Reset	⟨1⟩										
Initial Setting	—	⟨1⟩		0		—	-P				
Current Count Reset	—		⟨1⟩								
Count Enable	—			⟨1⟩							
Output Enable	—				⟨1⟩						
Current Count Preset	—					⟨1⟩	-P				
Notch Point Preset	—	—				—	⟨1⟩P				
Forward / Reverse Run Output	—				1			⟨1⟩			
Forced Notch Output 0 to 8	—				1				⟨1⟩ ⟨0⟩		
Monitor 0 to 3	—									⟨1⟩ ⟨0⟩ Combination	

Note : Symbols in table above mean the followings
1 : ON, 0 : OFF, ⟨1⟩ : OFF→ON, — : no status change, Blank space : disregarded,
-P : Not under notch point preset scanning,
⟨1⟩P : Under notch point preset scanning (see Par. 5.4.2)
①, ⟨1⟩, ⟨1⟩P : indicate coils which are made effective after conditions of other coils are met.
<How to read the table> The vertical column indicates the module operation, and the horizontal column indicates the corresponding output coil ON/OFF condition.

For example, when executing the B2802 initial setting, the output coil conditions are tracked horizontally:
① The coils for "module reset" and "current count preset" are free from status change.
② Notch point presetting is off.
③ The "count enable" coil is off.
Finally, "initial setting" coil is turned from OFF to ON.

5.3 INPUT RELAY (CONTROL SIGNAL) FOR B2802 TO CPU MODULE

(1) Input Relay List

The input relays activate as control signals from B2802 to the CPU module using 16 points (or 8 points). Table 5.5 shows the input relay list.

Table 5.5 Input Relay List

GL20	GL60S	Signal Name
1001 + 8n	10001 + 8n	READY
1002 + 8n	10002 + 8n	Preset ACK
1003 + 8n	10003 + 8n	Preset NAK
1004 + 8n	10004 + 8n	Carry
1005 + 8n	10005 + 8n	Borrow
1006 + 8n	10006 + 8n	Notch output 0
1007 + 8n	10007 + 8n	Notch output 1
1008 + 8n	10008 + 8n	Notch output 2
1009 + 8n	10009 + 8n	Notch output 3
1010 + 8n	10010 + 8n	Notch output 4
1011 + 8n	10011 + 8n	Notch output 5
1012 + 8n	10012 + 8n	Notch output 6
1013 + 8n	10013 + 8n	Notch output 7
1014 + 8n	10014 + 8n	Notch output 8
1015 + 8n	10015 + 8n	Reserved for future use
1016 + 8n	10016 + 8n	Scan time error

n=0, 1, 2····

Reference No. for input relay allocation

(2) Input Relay Contents

The 16-point input relay gives the control signals with the contents shown in Table 5.6.

Table 5.6 Input Relay Signal Name and Contents

Reference No.		Signal Name	Contents
GL20	GL60S		
1001 + 8n	10001 + 8n	READY	Shows result of module self-diagnosis. ON for normal, result, OFF for abnormal (e. g., errors in ROM, RAM, WDT and check). It stays OFF for approximately 0.5 sec for power ON, or module reset.
1002 + 8n	10002 + 8n	Preset ACK	Shows that B2802 preset operation has been completed normally. While preset command is ON, it stays on (initial setting, current count setting, notch point setting.)
1003 + 8n	10003 + 8n	Preset NAK	Indicates tha the preset operation in the B2802 is not working correctly. Stays ON while preset command is ON.
1004 + 8n	10004 + 8n	Carry	Turns ON for 1 scan when the current count changes to 0 after 999,999 (GL20) or 99,999,999 (GL60S).
1005 + 8n	10005 + 8n	Borrow	Turns ON for 1 scan when the current count gets smaller than 0 and changes to 999,999 (GL20) or 99,999,999 (GL60S).
1006 + 8n	10006 + 8n	Notch output 0	Indication of B2802's currently outputting external notch output. Notch output 0 ···→corresponding to N_0 (notch output 0) ⋮ ⋮ Notch output 8 ···→corresponding to N_8 (notch output 8) Effective when "output enable" coil is ON.
1007 + 8n	10007 + 8n	Notch output 1	
1008 + 8n	10008 + 8n	Notch output 2	
1009 + 8n	10009 + 8n	Notch output 3	
1010 + 8n	10010 + 8n	Notch output 4	
1011 + 8n	10011 + 8n	Notch output 5	
1012 + 8n	10012 + 8n	Notch output 6	
1013 + 8n	10013 + 8n	Notch output 7	
1014 + 8n	10014 + 8n	Notch output 8	
1016 + 8n	10016 + 8n	Scan time error	Turns ON when scan time of CPU module is too short for the B2802 internal process. OFF is normal.

5.3 INPUT RELAY (CONTROL SIGNAL) FOR B2802 TO CPU MODULE (Cont'd)

(3) Precautions on Input Relays

(a) The input relays for "Preset ACK" and "Preset NAK".

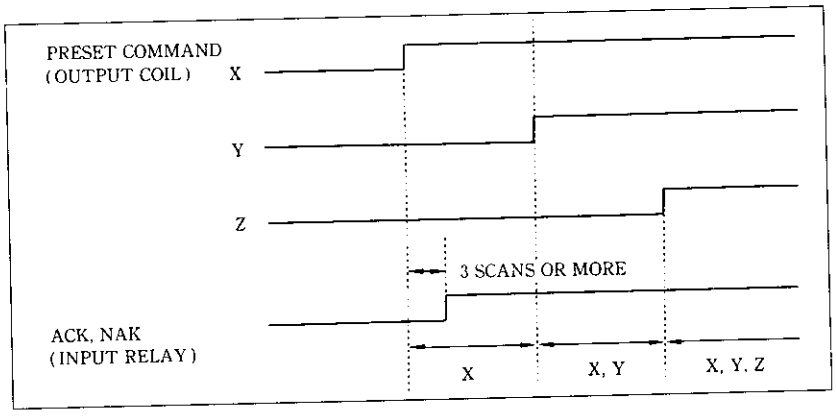


Fig. 5.1 Responses of Preset ACK and NAK (GL20)

5.4 OUTPUT REGISTERS (SETTING DATA) FOR CPU MODULE TO B2802

When presetting various setting data to the B2802 from a CPU module two or eight successive output registers are used. Preset commands which require output registers are ; "initial setting", "current count preset command", and "notch point preset command".

Since the same output registers are used for preset commands, care must be taken not to duplicate their timings. One output register will allow 3-digit decimal (GL20), or 4-digit decimal (GL60S). Table 5.7 shows allocations of output registers.

Table 5.7 Output Register Allocations (BINARY)

GL20	GL60S	Output Register No.	
4001 + n	40001 + n	1ST	2 Registers Allocated
4002 + n	40002 + n	2ND	
4003 + n	40003 + n	3RD	8 Registers Allocated
4004 + n	40004 + n	4TH	
4005 + n	40005 + n	5TH	
4006 + n	40006 + n	6TH	
4007 + n	40007 + n	7TH	
4008 + n	40008 + n	8TH	

n=0, 1, 2 ····

Reference No. for output register allocations

The selection between 2-register allocation and 8-register allocations made with the notch point setting mode.

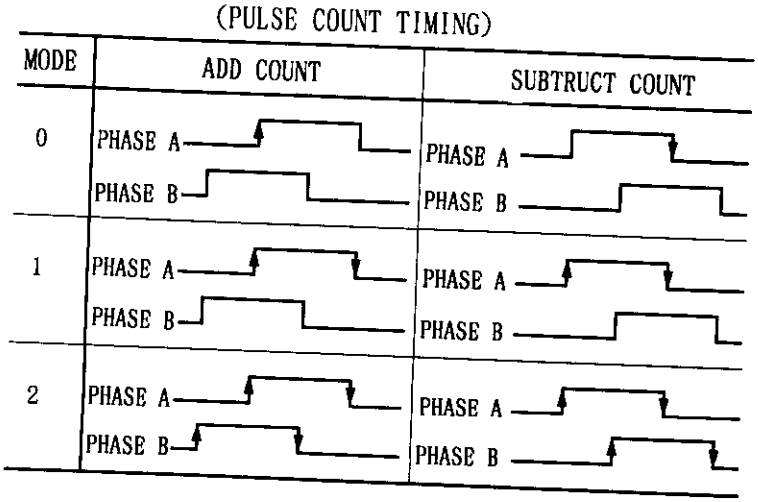
5.4.1 Initial Settings

Initial settings are used for setting counter functions of the B2802. Initial settings are achieved by setting an initial value to output registers and by output coil command "initial setting".

(1) Initial Setting Items

Table 5.8 shows initial setting items of the B2802.

Table 5.8 Initial Setting Items

Setting Items	Description
Pulse Input Mode Setting	Specifies pulse input mode 0 : Pulse with sign 1 : Phases A, B
Pulse Count Mode Setting (Phases A, B)	The setting pulse input mode and specifying phases A/B pulse count mode for phases A/B need to be specified. 0 : ×1 1 : ×2 2 : ×4 (PULSE COUNT TIMING) 
Notch Output Pattern Setting	Notch output patterns are set. 0 : Pattern A 1 : Pattern B
Hysteresis Width Setting	Notch output hysteresis width is specified. Setting is possible between 0 and 99 pulses.
Notch Point Setting Mode	Required number of notches and number of output registers are specified. Remember that when setting the number of notch points, the number of CPU module scans are also relevant. (see Par. 5.4.2) 0 : 1-notch point setting (2 output registers × 1 scan) 1 : 4-notch point setting (2 output registers × 2 scans) 2 : 4-notch point setting (8 output registers × 1 scan) 3 : 8-notch point setting (2 output registers × 8 scans) 4 : 8-notch point setting (8 output registers × 2 scans)

5.4.1 Initial Settings (Cont'd)

(2) Setting Initial Values to Output Registers

For the initial setting, two successive output registers are used. The setting method for the output registers is shown in Table 5.9. The values, in the frames are default values, which are automatically set when the power is turned on or the modules are reset.

Table 5.9 Setting Initial Values to Output Register

[GL20 □□□ (3 Digits), GL60S □□□□ (4 Digits)]

1ST

0 0 0 0

PULSE INPUT MODE SETTING
- 0 : SIGN + PULSE
- 1 : PHASES A and B

PHASES A and B PULSE INPUT MODE SETTING
- 0 : 1 MULTIPLIER
- 1 : 2 MULTIPLIERS
- 2 : 4 MULTIPLIERS

When sign + pulse input is specified, single multiplier is automatically selected and this position becomes idle.

NOTCH OUTPUT MODE SETTING
- 0 : PATTERN A
- 1 : PATTERN B

2ND

0 0 0 0

HYSTERESIS WIDTH SETTING
0 TO 99 PULSES

NOTCH POINT SETTING MODE
- 0 : 1-NOTCH POINT SETTING (2 OUTPUT REGISTERS × 1 SCAN)
- 1 : 4-NOTCH POINT SETTING (2 OUTPUT REGISTERS × 2 SCANS)
- 2 : 4-NOTCH POINT SETTING (8 OUTPUT REGISTERS × 1 SCAN)
- 3 : 8-NOTCH POINT SETTING (2 OUTPUT REGISTERS × 8 SCANS)
- 4 : 8-NOTCH POINT SETTING (8 OUTPUT REGISTERS × 2 SCANS)

< Precautions in initial setting processing >

(a) When the initial setting is executed,
- The counter current count is cleared.
- The notch point preset value is cleared, and the notch outputs are all turned off.
- The current count and preset value are cleared.
- The preset error is cleared.

(b) The initial setting checks all the set items for normal and abnormal values. When abnormal values are detected, they remain unchanged, and all other items are replaced by new setting values. Then, "PRESET NAK" turns on.

(c) The unused digit positions are invalid. Although values are displayed on the monitor, they are disregarded.

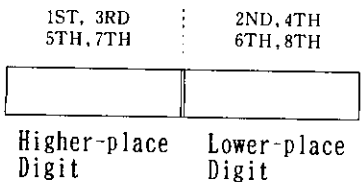
5.4.2 Data Setting

(1) Setting Method to Output Registers

Table 5.10 shows the data setting method for executing various preset commands to the output registers.

Table 5.10 Various Data Settings

Set Item		Output Register	
		GL20	GL60S
Current Count Preset		1ST 2ND 0 to 999,999	1ST 2ND 0 to 99,999,999
Notch Point Preset	2-reg. Allocation	1ST 2ND 0 to 999,999	1ST 2ND 0 to 99,999,999
	8-reg. Allocation	1ST 2ND 3RD 4TH 5TH 6TH 7TH 8TH 0 to 999,999	1ST 2ND 3RD 4TH 5TH 6TH 7TH 8TH 0 to 99,999,999

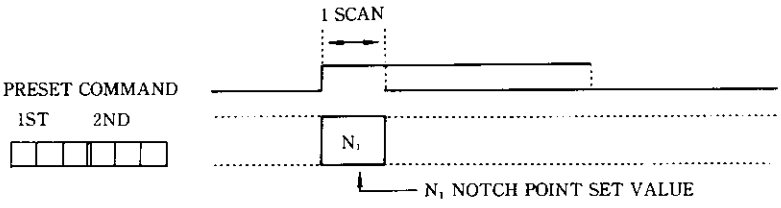
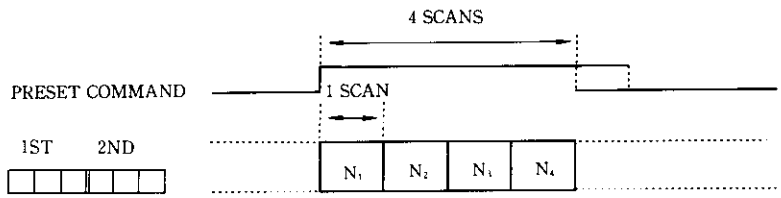
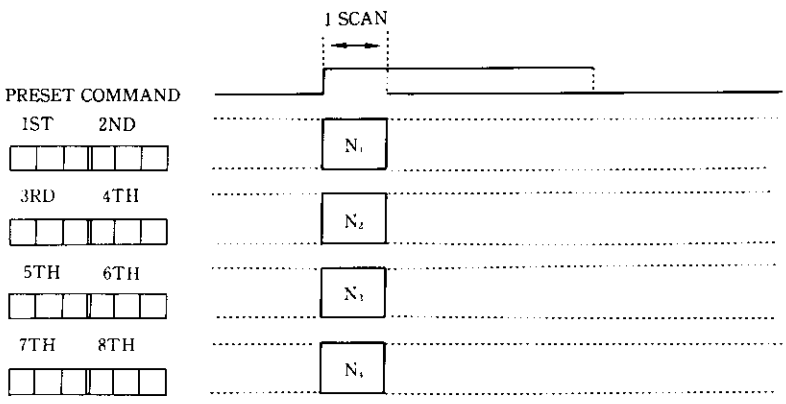
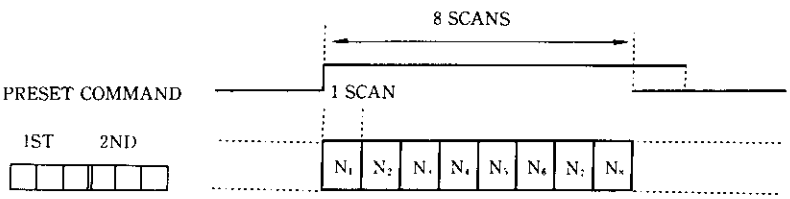
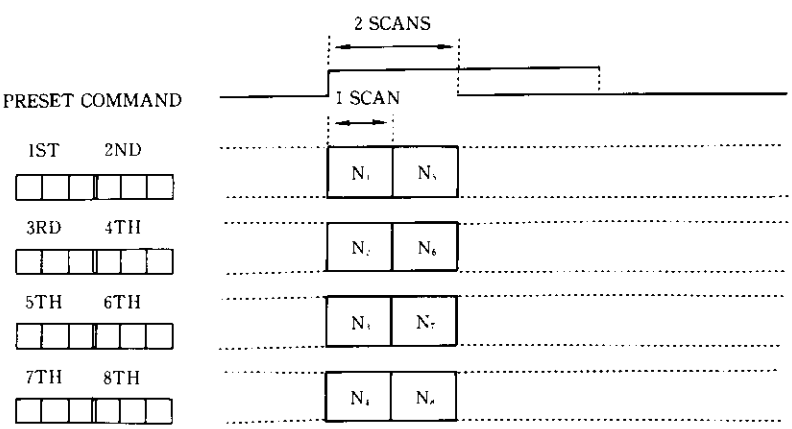


5.4.2 Data Setting (Cont'd)

(2) Notch Point Preset Sequence by Notch Point Setting Mode

For the notch point setting, preset sequences are specified for the setting modes. The output register contents must be controlled in accordance with Table 5.11. Refer to the preset ladder circuit examples in Par. 5.6.

Table 5.11 Notch Point Preset Sequence (Example of GL20)

Notch Point Setting Mode		Notch Point Preset Sequence
0	1-Notch Point Setting : 2-Output Register × 1 Scan	
1	4-Notch Point Setting : 2-Output Register × 4 Scans	
2	4-Notch Point Setting : 8-Output Register × 1 Scan	
3	8-Notch Point Setting : 2-Output Register × 8 Scans	
4	8-Notch Point Setting : 2-Output Register × 2 Scans	

5.5 INPUT REGISTER (MONITOR DATA) FOR B2802 TO CPU MODULE

To monitor various data of B2802, two contiguous input registers are used. The contents of the monitored data vary with monitor code (output coil: monitor 0 to 3 ON/OFF combination) setting.

Table 5.12 Input Register Allocation (Binary)

GL20	GL60S	Input Register No.
3001 + n	30001 + n	1ST
3002 + n	30002 + n	2ND

n=0, 1, 2 ····

Reference No. for Input Register Allocation

Table 5.13 Monitor Contents of Input Registers

Monitor Contents	Input Registers	
	GL20	GL60S
Current Count/ Current Count Preset Value/ Notch Point Set Value	1ST 2ND 0~999, 999	1ST 2ND 0~99, 999, 999
Initial Setting Value	Same form as output register of the initial setting value (see Table 5.9).	

Table 5.14 Monitor Code and Monitor Contents

Monitor 0	Monitor 1	Monitor 2	Monitor 3	Contents
0	0	0	0	Current count
1	0	0	0	N_1 notch point set value
0	1	0	0	N_2 notch point set value
1	1	0	0	N_3 notch point set value
0	0	1	0	N_4 notch point set value
1	0	1	0	N_5 notch point set value
0	1	1	0	N_6 notch point set value
1	1	1	0	N_7 notch point set value
0	0	0	1	N_8 notch point set value
1	0	0	1	Initial set value
0	1	0	1	Current count preset value

1:ON, 0:OFF

Combinations other than the above bring the counter to the current count.

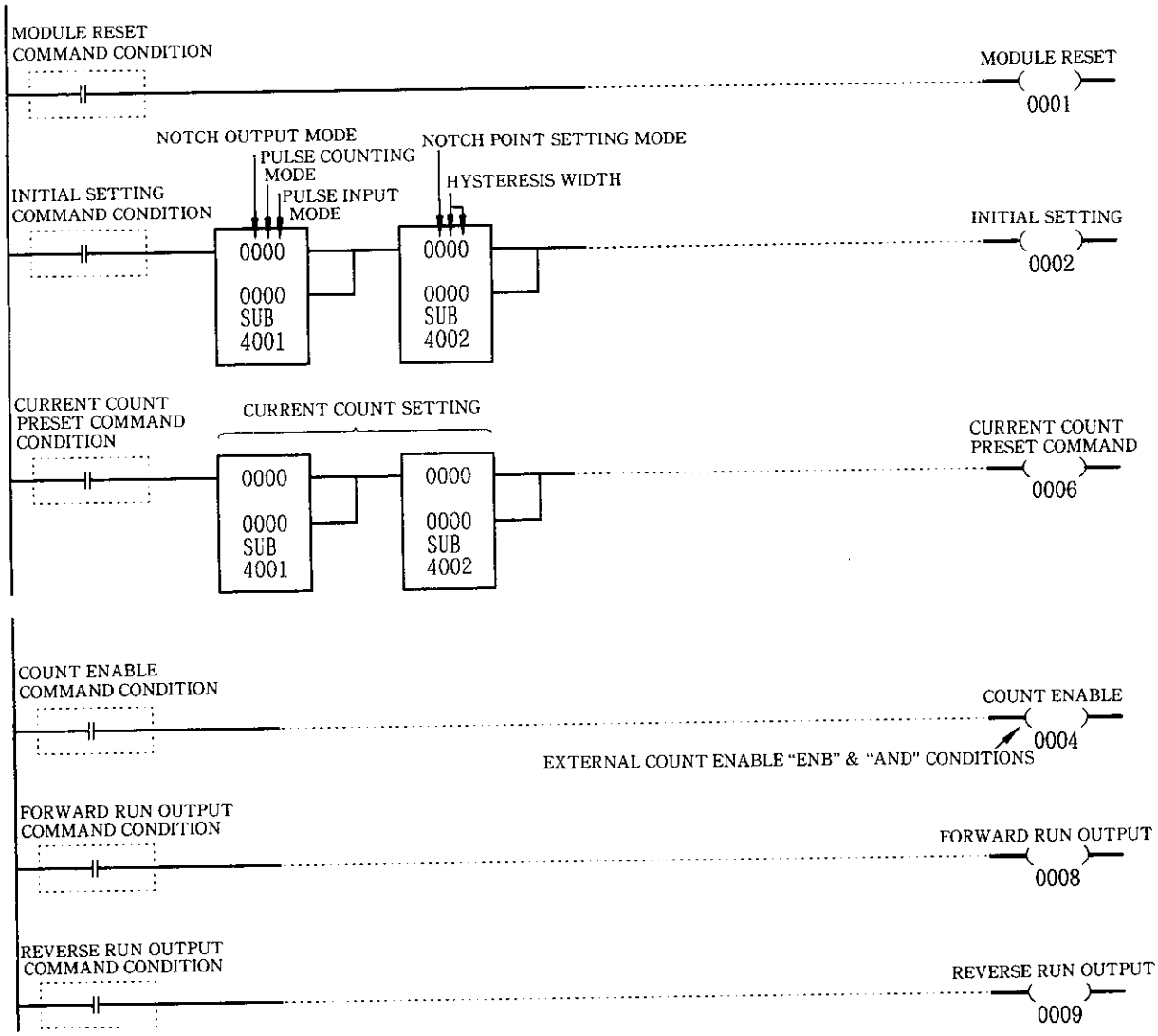
5.6 LADDER CIRCUIT EXAMPLES

5.6.1 6-Digit GL20 Circuit Examples

(1) Various Settings

Output register: 4001, 4002 } Allocation

Output coil: 0001 to 0024

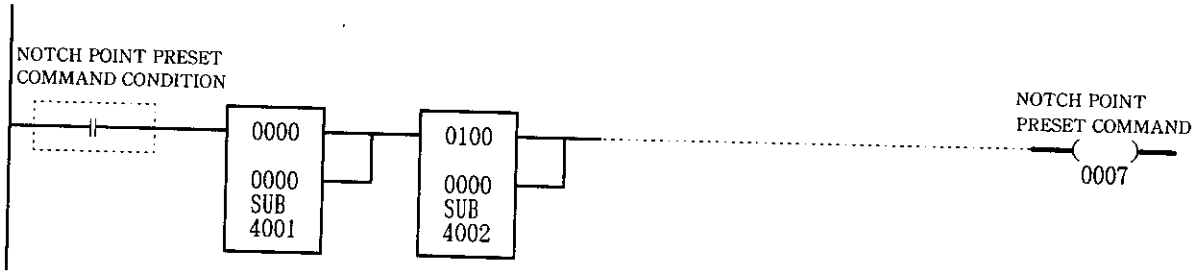


(2) 1-Notch Point Setting, 2 Output Registers × 1 Scan Example

Output coil: 0001 to 0024

Output registers: 4001, 4002 } Allocation

N_1 notch point setting value is 100.

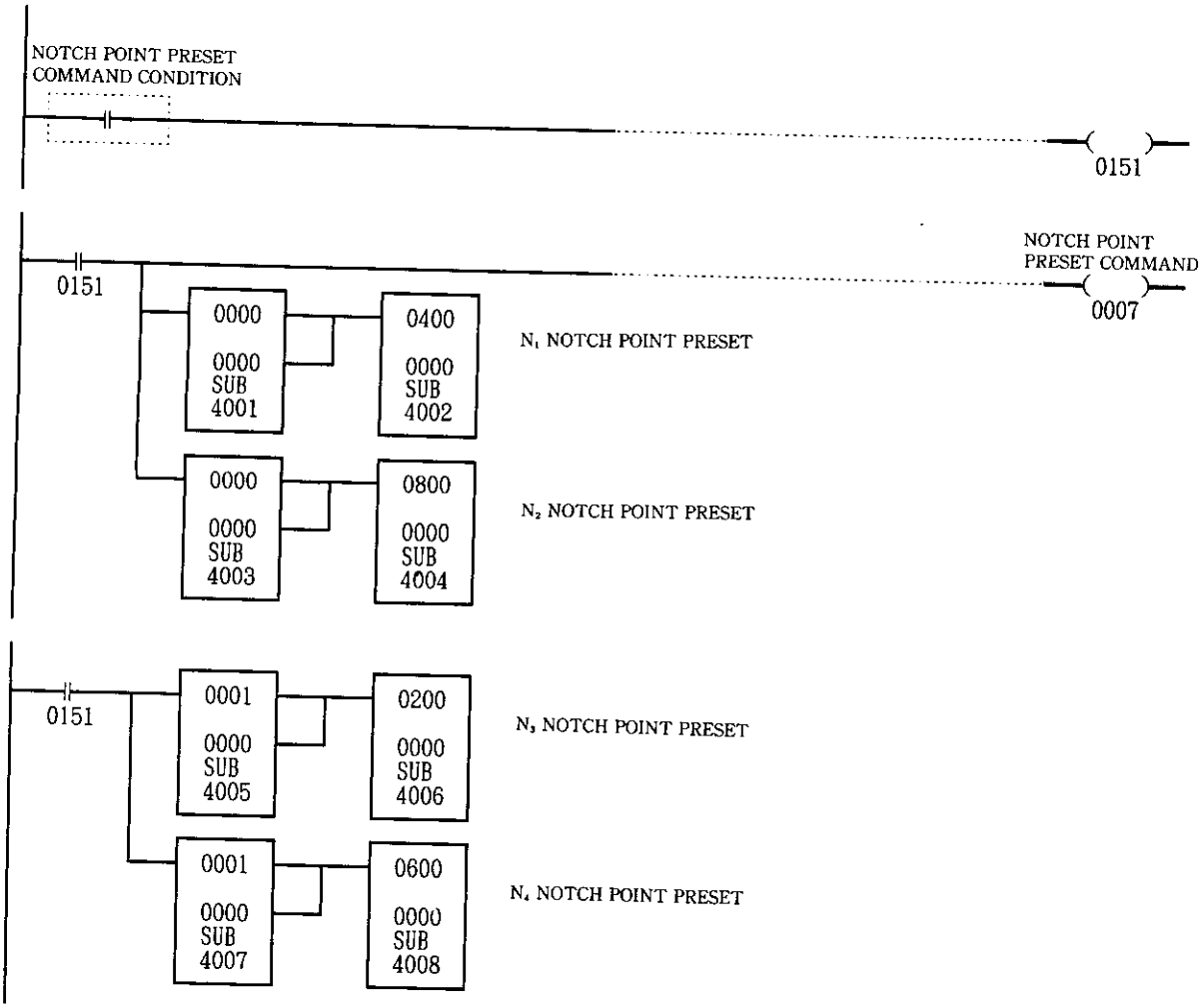


(3) 4-Notch Point Setting, 8 Output Registers × 1 Scan Example

Output coil: 0001 to 0024

Output Register: 4001, 4002 ····4008 } Allocation

N_1 notch point is set to 400,
N_2 notch point is set to 800,
N_3 notch point is set to 1200
N_4 notch point is set to 1600

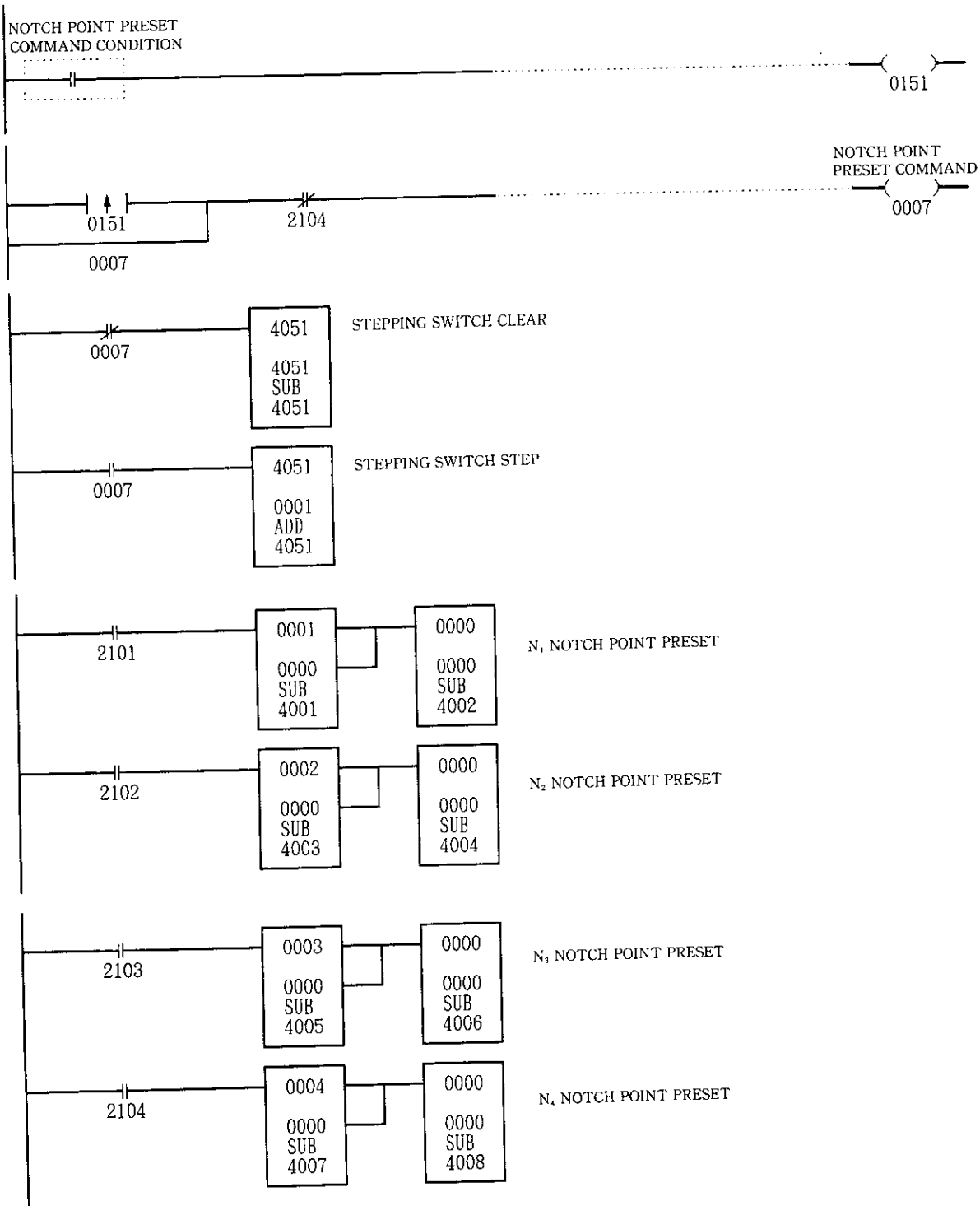


5.6.1 6-Digit GL20 Circuit Examples (Cont'd)

(4) 4-Notch Point Setting, 2 Output Registers × 4 Scans Example

Output coil: 0001 to 0024
Output register: 4001, 4002, 4051
} Allocation

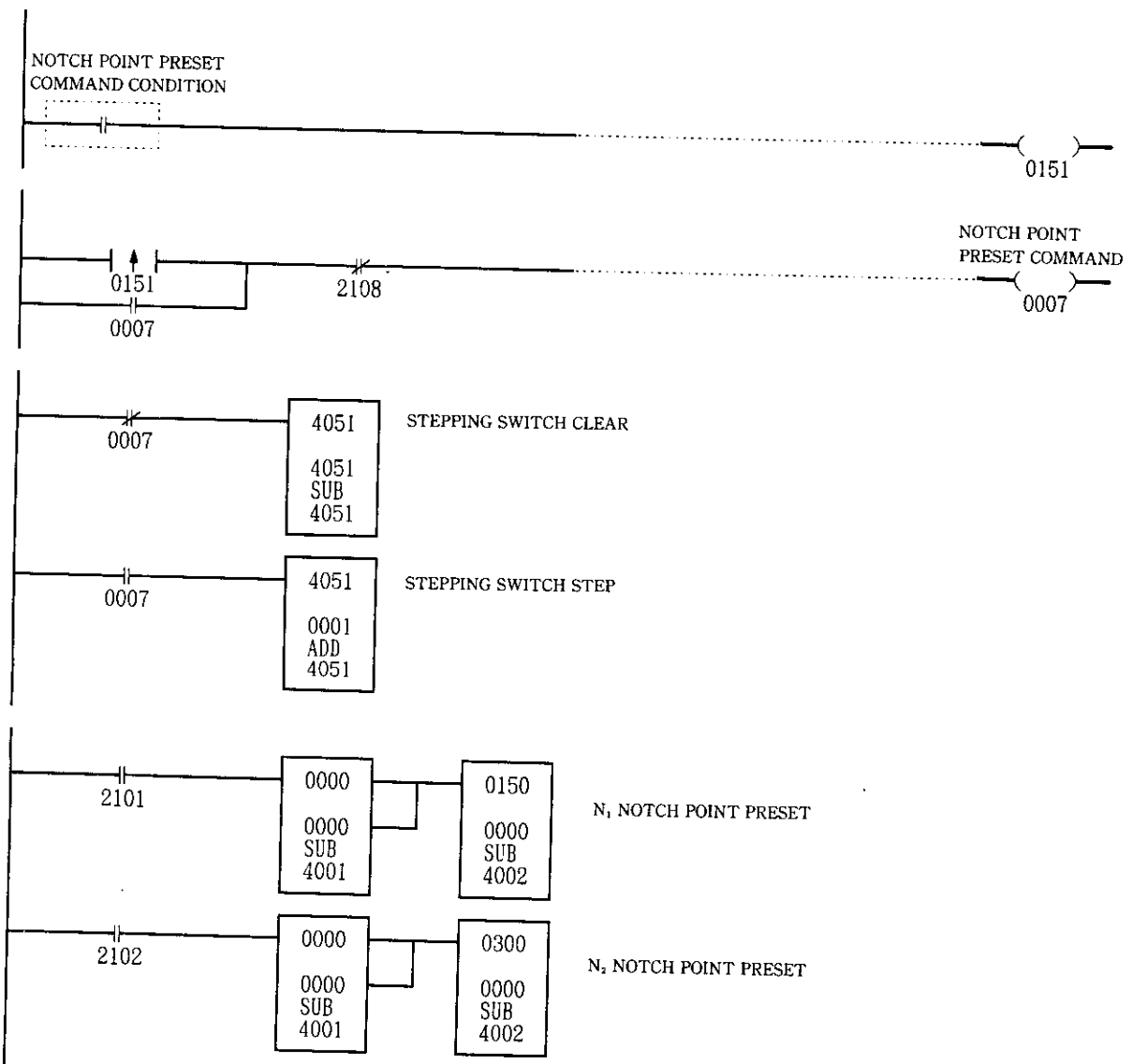
N_1 notch point is set to 1000
N_2 notch point is set to 2000
N_3 notch point is set to 3000
N_4 notch point is set to 4000



(5) 8-Notch Point Setting, 2 Output Registers × 8 Scans Example

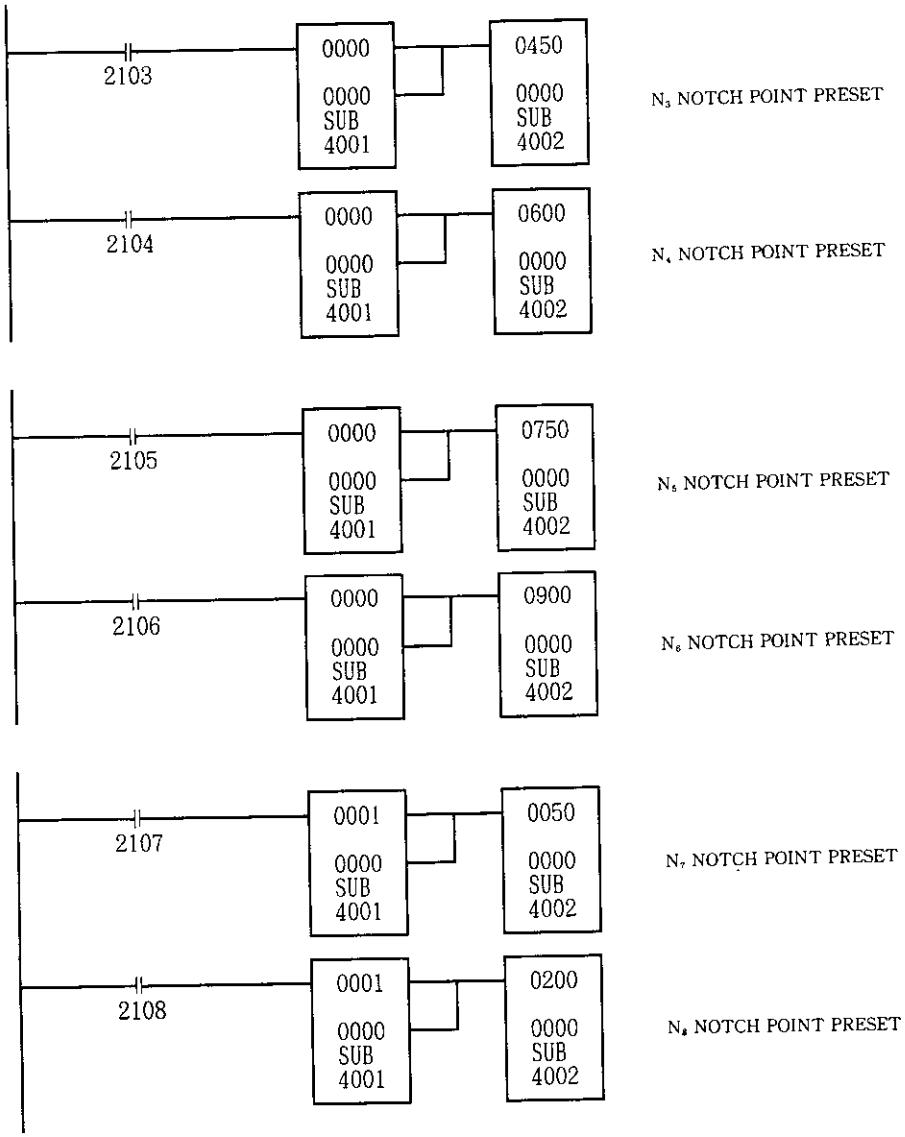
Output coil: 0001 to 0024
Output register: 4001, 4002
} Allocation

N_1 notch point is set to 150
N_2 notch point is set to 300
N_3 notch point is set to 450
N_4 notch point is set to 600
N_5 notch point is set to 750
N_6 notch point is set to 900
N_7 notch point is set to 1050
N_8 notch point is set to 1200



5.6.1 6-Digit GL20 Circuit Examples (Cont'd)

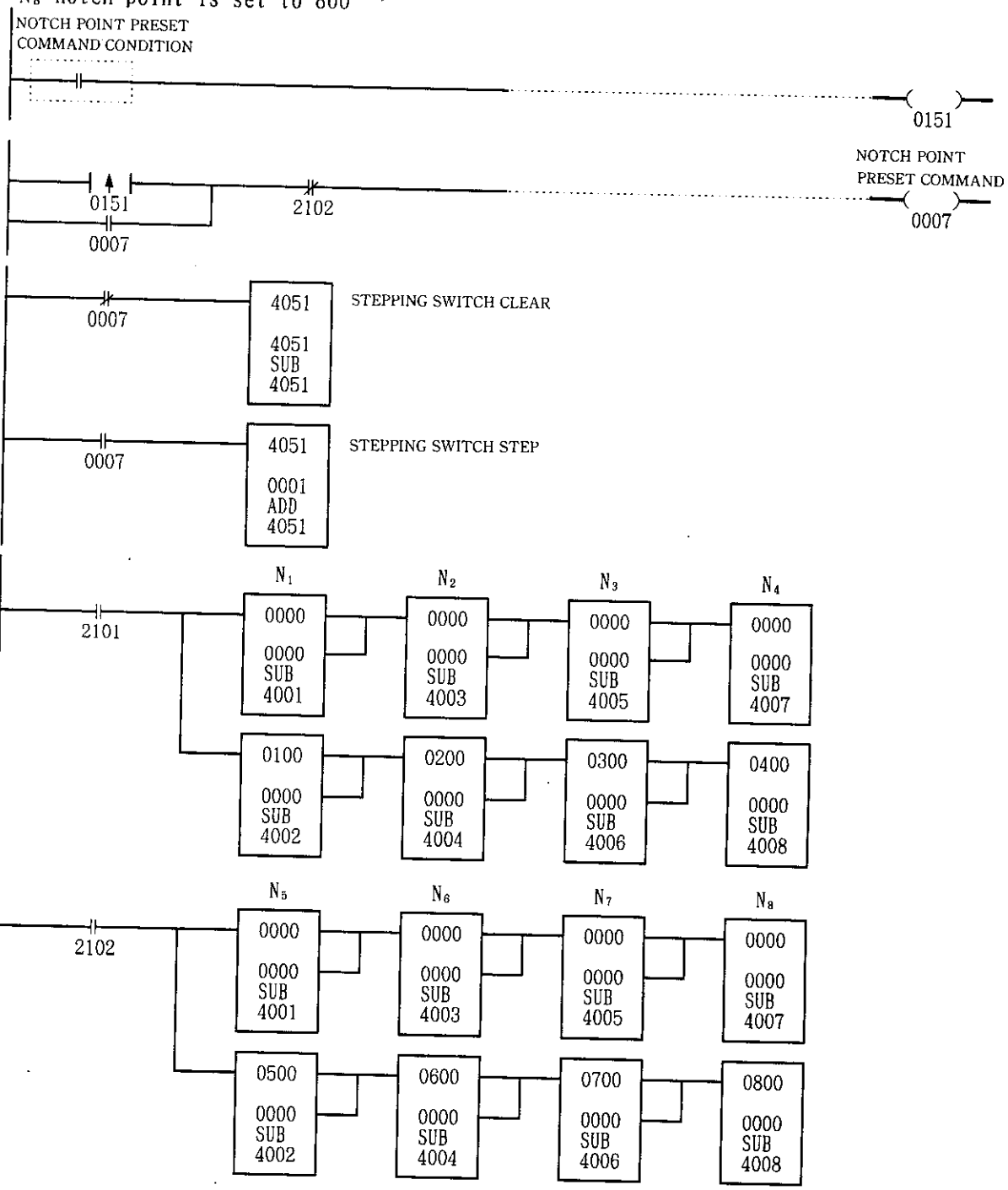
(5) 8-Notch Point Setting, 2 Output Registers × 8 Scans Example (Cont'd)



(6) 8-Notch Point Setting, 8 Output Registers × 2 Scans Example

Output coil: 0001 to 0024
Output register: 4001 to 4008
} Allocation

N_1 notch point is set to 100
N_2 notch point is set to 200
N_3 notch point is set to 300
N_4 notch point is set to 400
N_5 notch point is set to 500
N_6 notch point is set to 600
N_7 notch point is set to 700
N_8 notch point is set to 800



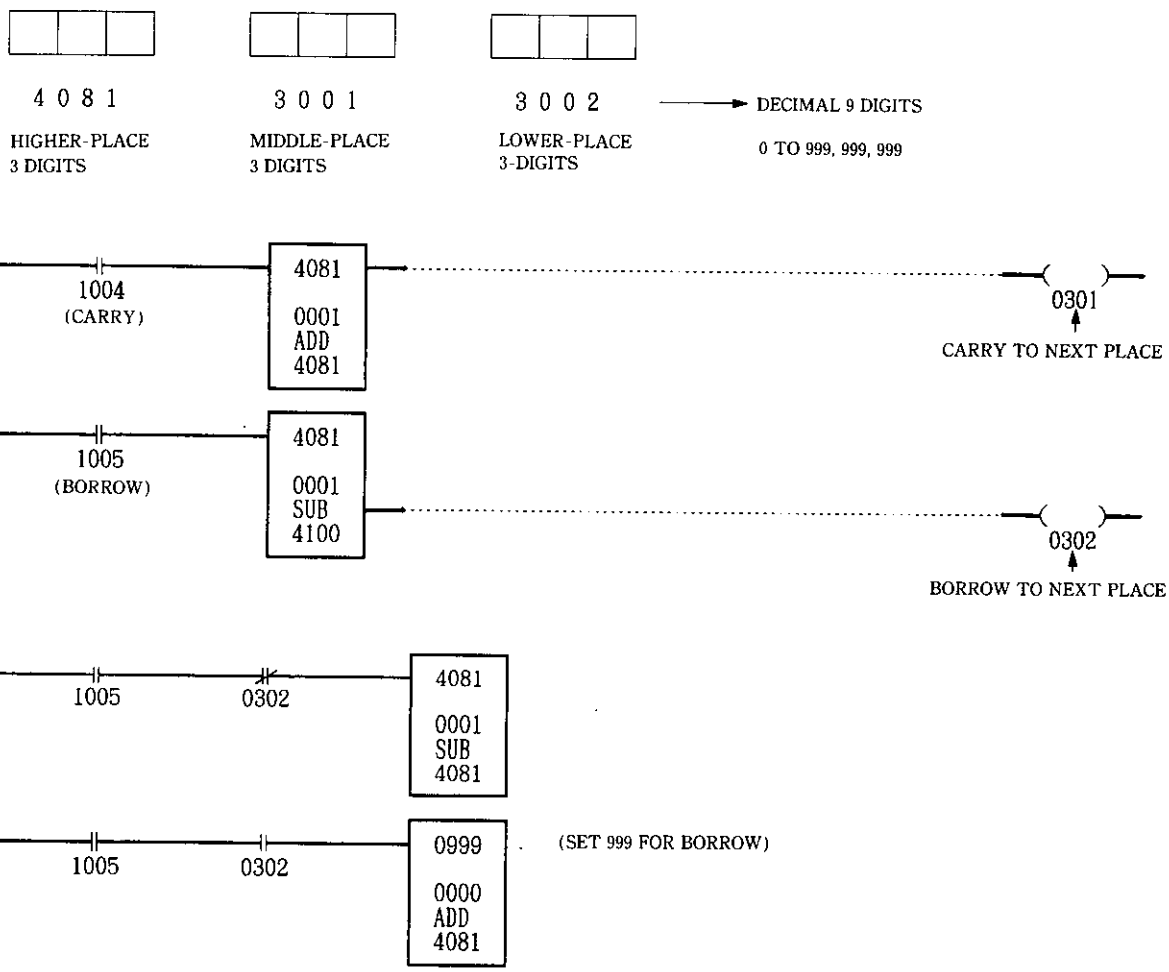
5.6.1 6-Digit GL20 Circuit Examples (Cont'd)

(7) Carry and Borrow Circuit Example

When the number of counting digits are more than 6, digits can be carried or borrowed from the module.

Input relay: 1001 to 1016
Input register: 3001, 3002
} Allocation

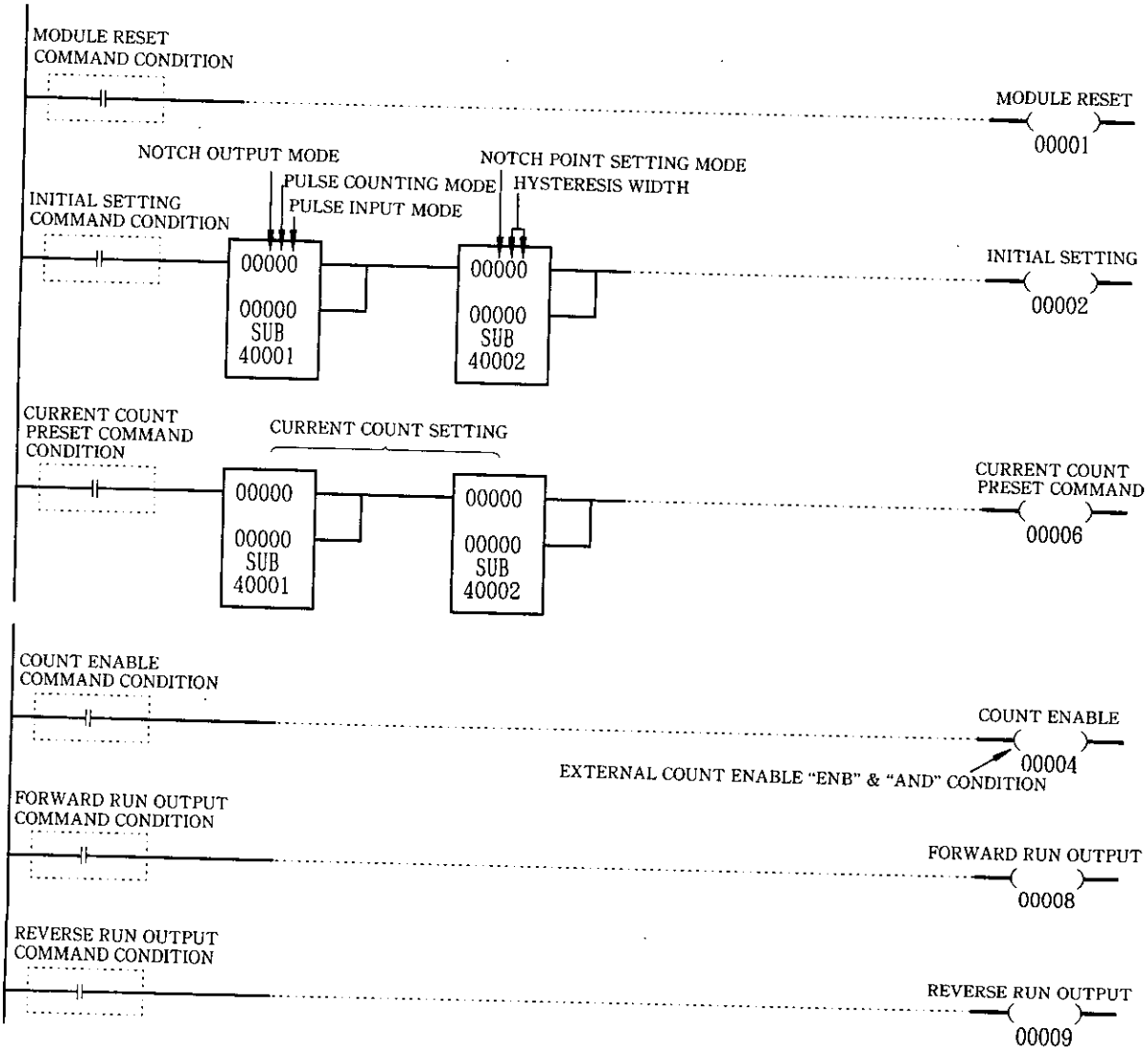
Higher-place digit register: 4081
Working register: 4100
}



5.6.2 8-Digit GL60S Ladder Circuit Examples

(1) Various Settings

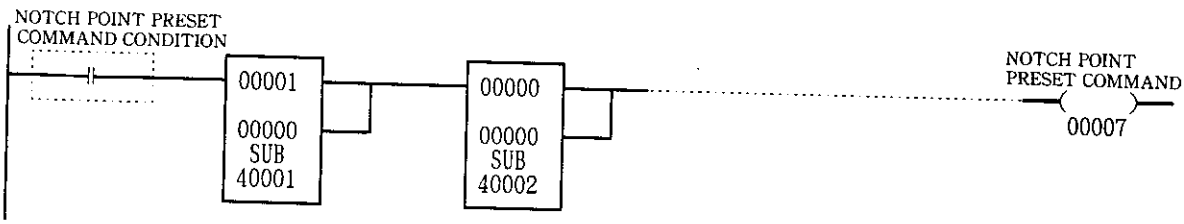
Output coil: 00001 to 00024
Output register: 40001, 40002 } Allocation



(2) 1-Notch Point Setting, 2 Output Registers × 1 Scan Example

Output coil: 00001 to 00024
Output register: 40001, 40002 } Allocation

N_1 notch point is set to 10000.



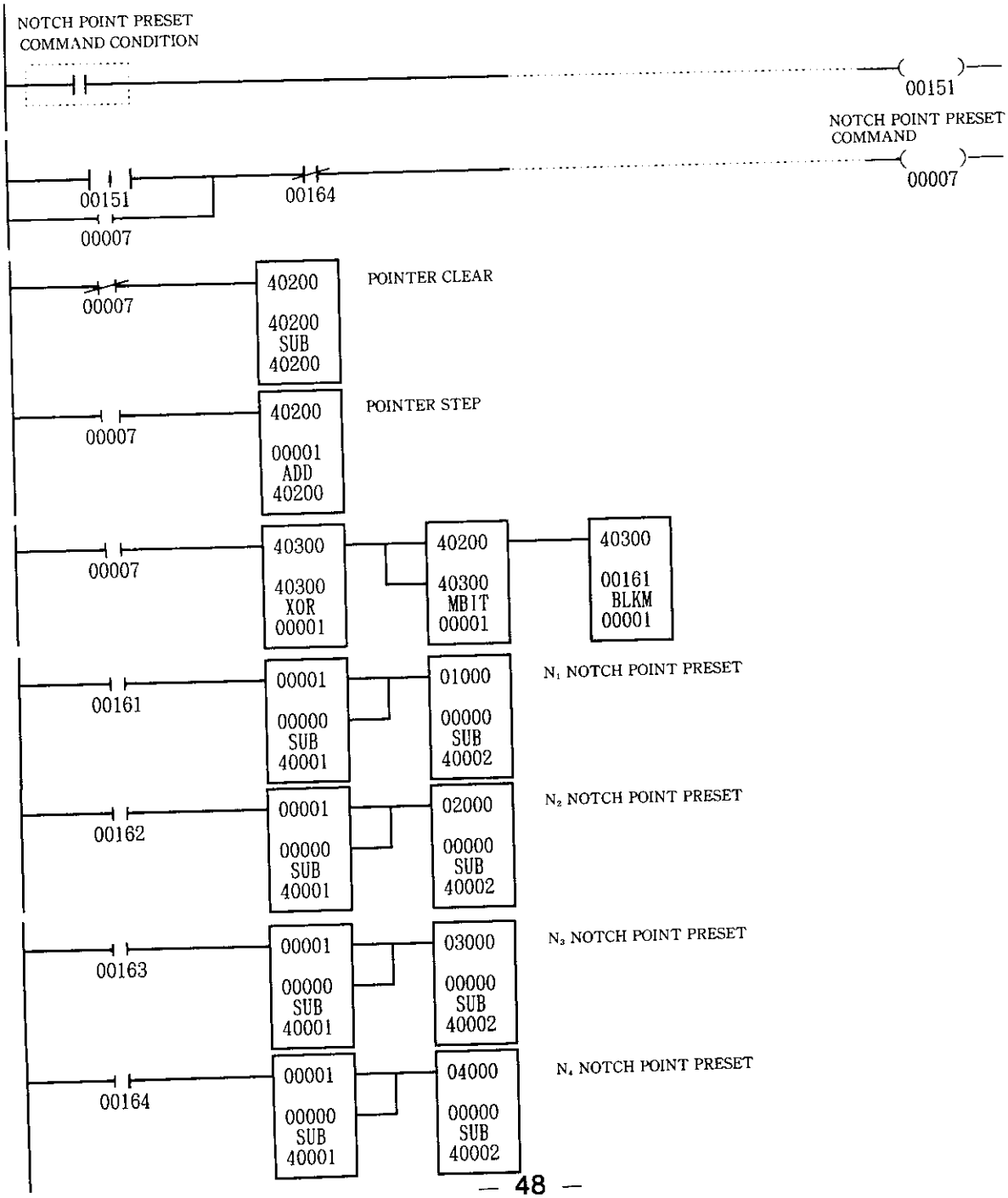
5.6.2 8-Digit GL60S Ladder Circuit Examples (Cont'd)

(3) 4-Notch Point Setting, 2 Output Registers × 4 Scans Examples

Output coil: 00001 to 00024
Output register: 40001, 40002 } Allocation

40200: Pointer
40300: Working register

N_1 notch point is set to 11000
N_2 notch point is set to 12000
N_3 notch point is set to 13000
N_4 notch point is set to 14000



(4) 8-Notch Point Setting, 8-Registers × 2 Scans Example

Output coil: 00001 to 00024

Output register: 40001 to 40008 } Allocation

40200: Pointer

40300: Working register }

40101: set N_1 notch point to 500

40103: set N_2 notch point to 2500

40105: set N_3 notch point to 4500

40107: set N_4 notch point to 6500

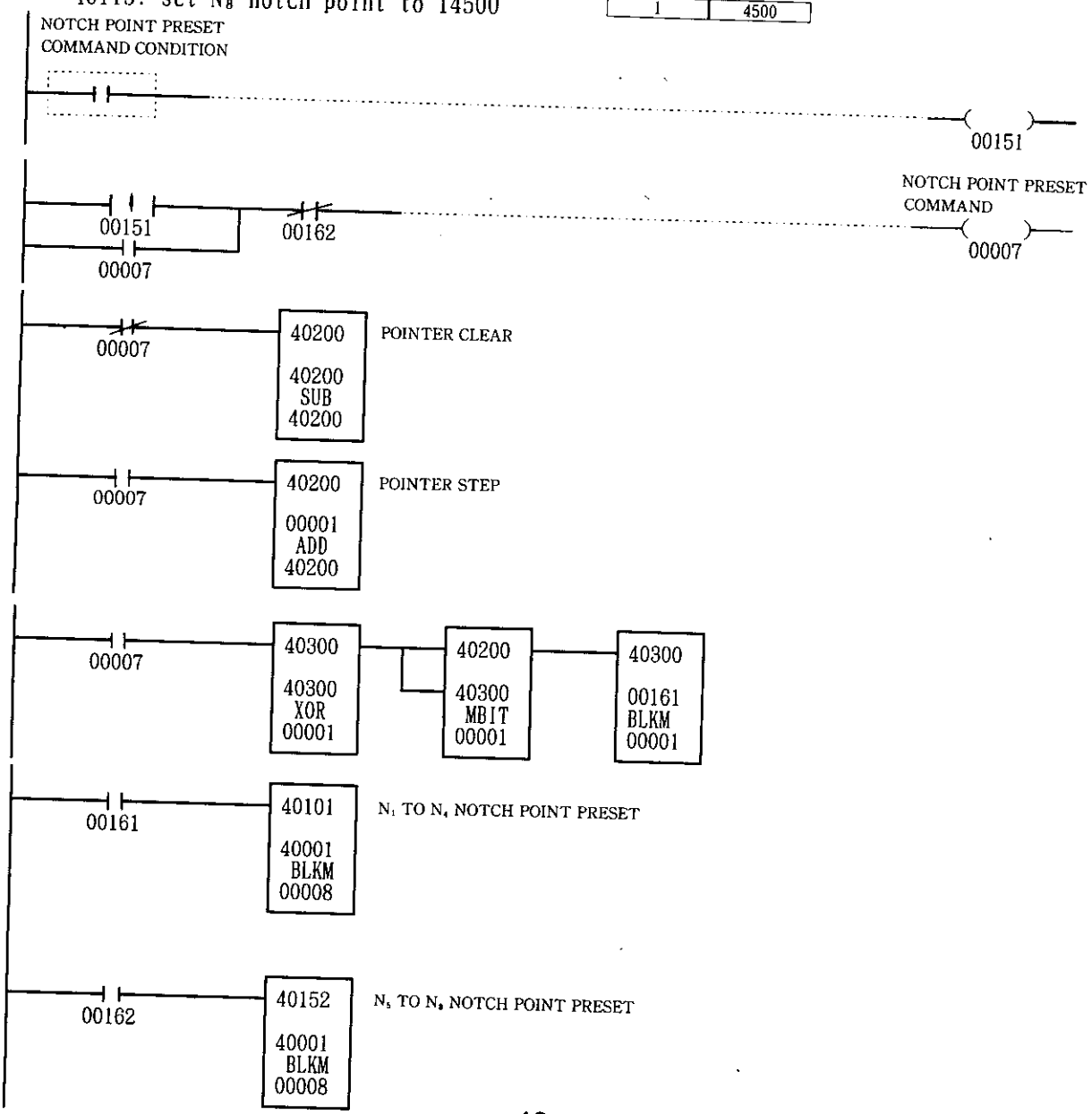
40109: set N_5 notch point to 8500

40111: set N_6 notch point to 10500

40113: set N_7 notch point to 12500

40115: set N_8 notch point to 14500

40101	40102
0	500
40103	40104
0	2500
40105	40106
0	4500
40107	40108
0	6500
40109	40110
0	8500
40111	40112
1	500
40110	40114
1	2500
40115	40116
1	4500



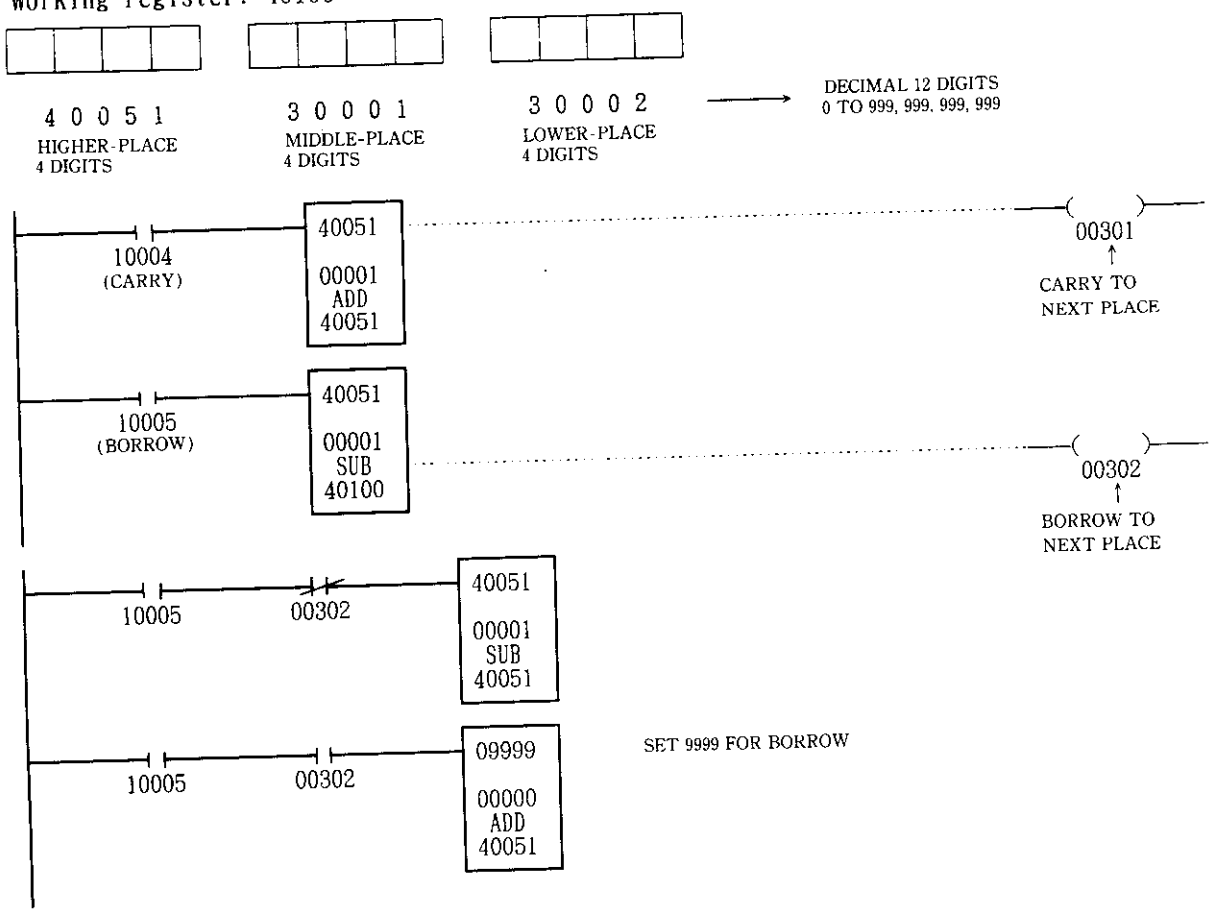
5.6.2 8-Digit GL60S Ladder Circuit Examples (Cont'd)

(5) Carry and Borrow Circuit Example

When 8 counting digits are not sufficient, digits may be increased by carry and borrow calculations from the module.

Input relay: 10001 to 10016
Input register: 30001, 30002
} Allocation

Higher place register: 40051
Working register: 40100



6. EXTERNAL INTERFACE

6.1 B2802 FRONT PANEL ARRANGEMENT

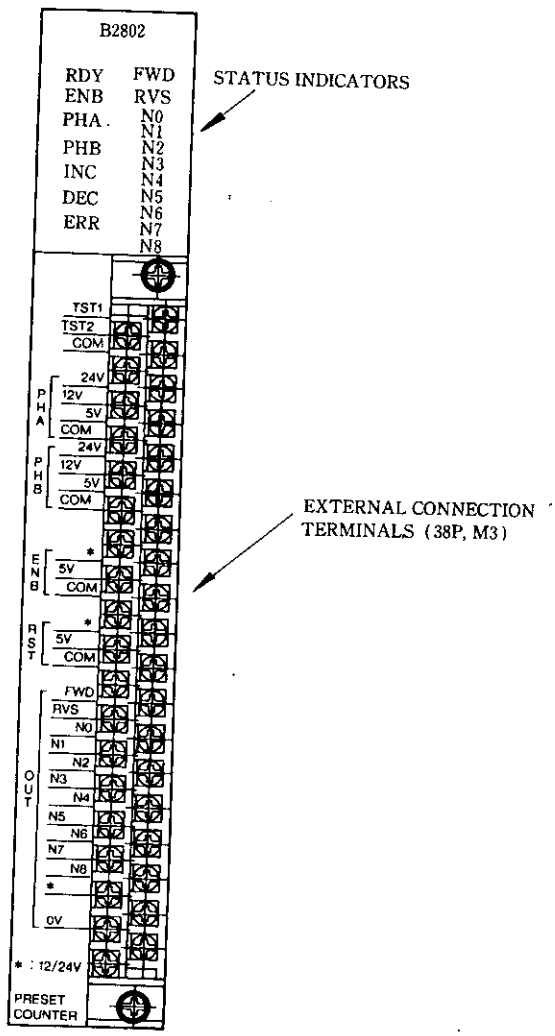


Fig. 6.1 B2802 Front Panel Arrangement

6.2 I/O SIGNAL APPLICATIONS

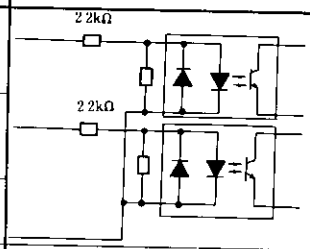
(1) I/O Signals and Description

Table 6.1 I/O Signals and Description

Signal Names	Description
TST1 (Add Test Input) TST2 (Subtract Test Input)	Test input terminals for simple count checking. TST1 is used for count test for ADD direction, and TST2 for SUBTRACT direction. Turn output coil "count enable" ON for ADD/SUBTRACT tests. External pulse input count should be stopped in the test modes (refer to Table 6.3). "□ENB" can be at OFF.
PHA (Phase A : 24, 12, 5V) PHB (Phase B : 24, 12, 5V)	Pulses fed to phase A and B terminals are counted as current counter values. Select 24V, 12V or 5V terminals depending on the voltage level of signals. Either pulse system for phase A and B, or sign with pulse system can be selected for the input system. For the pulse with sign system, feed the sign to phase B and the pulse to phase A. For the pulse system for phases A and B a pulse count mode of ×1, ×2, and ×4 can be selected. The sign with pulse system is good for an ×1 count only. These selections are made by initial settings. (Refer to Table 6.4)
ENB (External Count Enable Input)	Input signal to enable the counter to count. Count can be made when "ENB" is ON and at the same time output coil "count enable" is ON.
RST (External Reset Input)	While "RST" is ON counter current value is reset. Pulse count is stopped. It forms an OR condition with the output coil "current value reset".
FWD (External Forward Run Output) RVS (External Reverse Run Output)	The ON/OFF status of the external coil "FWD" and "RVS" is output as it is. These signals are effective when output coil "output enable" is ON.
N_0(external notch output 0) N_1(external notch output 1) N_2(external notch output 2) N_3(external notch output 3) N_4(external notch output 4) N_5(external notch output 5) N_6(external notch output 6) N_7(external notch output 7) N_8(external notch output 8)	Output based on the comparison between the notch point set value and the counter current count. Forced notch output, if any, is output with priority. These signals are effective when the output coil "output enable" is ON.

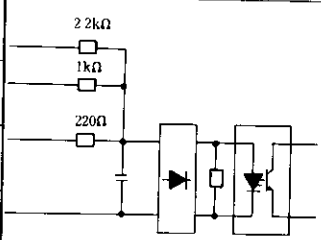
(2) I/O Signals and Electrical Characteristics

Table 6.2 I/O Signals and Electrical Specifications

	Signal Name	Counter Terminal No.	Internal Circuit	Electrical Specification
	TST 1 (ADD Test Input)	1		
	TST 2 (SUBTRACT Test Input)	2		
	COM	3		

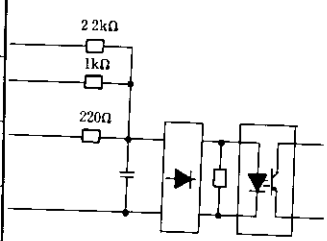
	Operation Voltage	Operation Current
ON	10.2 to 26.4V	4 to 12mA
OFF	3V or less	0.5mA or less

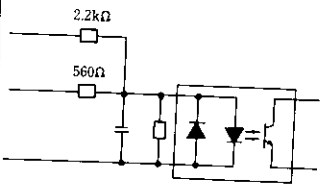
ON Response Time: 120ms or less
OFF Response Time: 120ms or less

PHA	24V (Phase A Pulse Input)	5	
	12V (Phase A Pulse Input)	6	
	5V (Phase A Pulse Input)	7	
	COM	8	

		Operation Voltage	Operation Current
24V	ON	20.4 to 26.4V	7 to 11mA
	OFF	3V or less	0.3mA or less
12V	ON	10.2 to 13.2V	7 to 11mA
	OFF	2V or less	0.3mA or less
5V	ON	4.5 to 5.5V	7 to 11mA
	OFF	1V or less	0.3mA or less

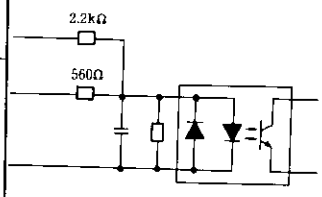
Phase A becomes pulse and phase B becomes sign at "sign + pulse" input mode.
- Max No. of input pulses:
  50 kpps (x1)
  100 kpps (x2)
  200 kpps (x4)

PHB	24V (Phase B Pulse Input)	9	
	12V (Phase B Pulse Input)	10	
	5V (Phase B Pulse Input)	11	
	COM	12	

ENB	*(12/24V) (External Count Enable Input)	15	
	5V (External Count Enable Input)	16	
	COM	17	

		Operation Voltage	Operation Current
12/24V	ON	10.2 to 26.4V	4 to 12mA
	OFF	3V or less	0.5mA or less
5V	ON	4.5 to 5.5V	6 to 7.5mA
	OFF	1V or less	0.5mA or less

ON Response Time : 1ms or less
OFF Response Time : 2ms or less

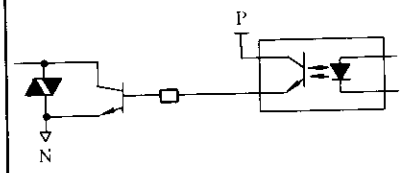
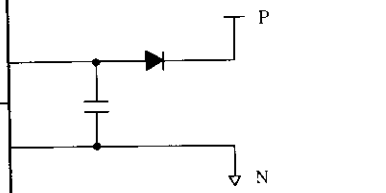
RST	*(12/24V) (External Reset Input)	19	
	5V (External Reset Input)	20	
	COM	21	

	Operation Voltage	Operation Current
ON	10.2 to 26.4V	4 to 12mA
OFF	3V or less	0.5mA or less

(OFF to ON Response Time)
External Count Enable : 1ms or less
External Reset : 6ms or less
(ON to OFF Response Time)
External Count Enable : 2ms or less
External Reset : 4ms or less

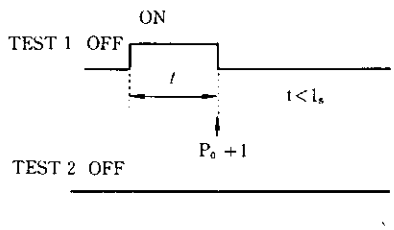
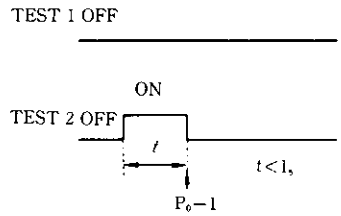
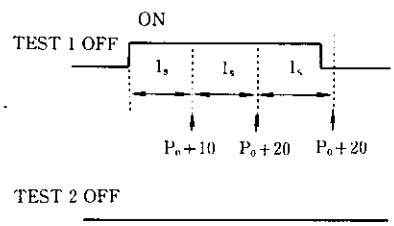
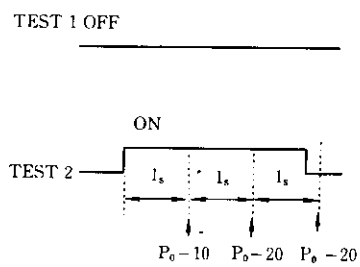
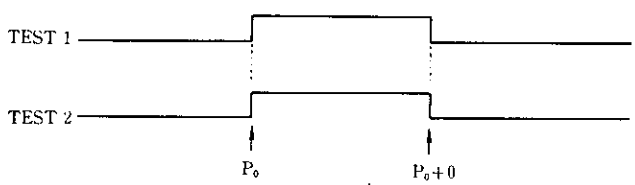
6.2 I/O SIGNAL APPLICATIONS (Cont'd)

Table 6.2 I/O Signals and Electrical Specifications

Signal Name	Counter Terminal No.	Internal Circuit	Electrical Specification
FWD (Extenal Forward Run Output	23		EXTERNAL OUTPUT Open collector output is effective at negative logic L. Max. load voltage : 29V ON voltage : 1.5V max. load current : 0.6A / 4 circuits. 0.25A / 1 circuit Peak surge current : 1A (10ms) OFF current : 0.2 mA max. Response time from pulse input to notch output : 5 ms max.
RVS (Extenal Reverse Run Output	24	SAME CIRCUIT AS ABOVE	
N_0 (External Notch Output 0)	25	SAME CIRCUIT AS ABOVE	
N_1 (External Notch Output 1)	26	SAME CIRCUIT AS ABOVE	
N_2 (External Notch Output 2)	27	SAME CIRCUIT AS ABOVE	
N_3 (External Notch Output 3)	28	SAME CIRCUIT AS ABOVE	
N_4 (External Notch Output 4)	29	SAME CIRCUIT AS ABOVE	
N_5 (External Notch Output 5)	30	SAME CIRCUIT AS ABOVE	
N_6 (External Notch Output 6)	31	SAME CIRCUIT AS ABOVE	
N_7 (External Notch Output 7)	32	SAME CIRCUIT AS ABOVE	
N_8 (External Notch Output 8)	33	SAME CIRCUIT AS ABOVE	
*(12/24) Power Supply Input for Output	34		Power supply voltage range : 10.2~26.4V Power supply:With all points ON, 40mA/24VDC, 20mA/12VDC
0V (For Output)	36		

(3) Test Input Count Timing

Table 6.3 TEST1 and TEST2 Count Timing

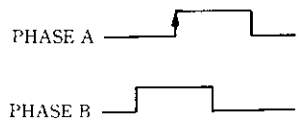
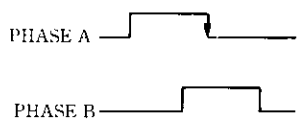
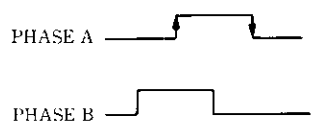
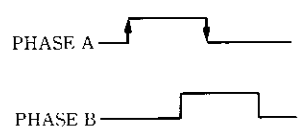
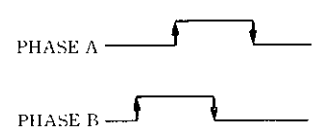
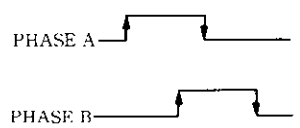
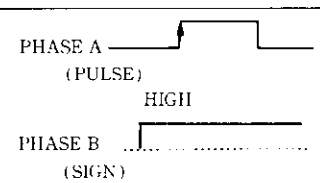
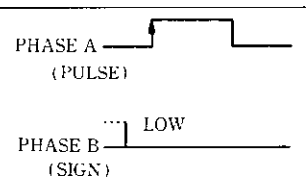
	ADD	SUBTRACT
① If ON time is less than one sec it becomes one-pulse ADD/SUBTRACT.		
② If ON time is more than one sec it becomes ten-pulse ADD/SUBTRACT.		
③ If TEST1 and TEST2 are simultaneously ON, count is stopped.		

Note:
1. Output coil "count enable" should be ON for test input mode. "ENB" off is possible.
2. "P_0" shows initial values.

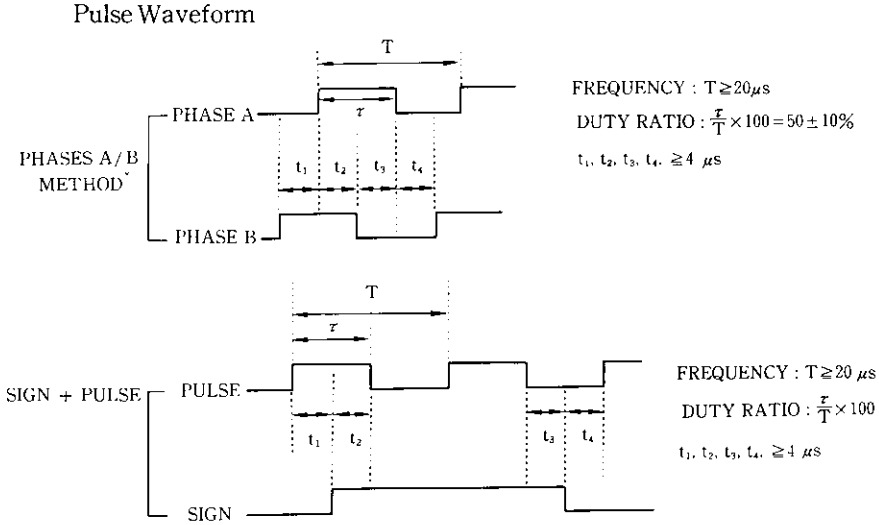
6.2 I/O SIGNAL APPLICATIONS (Cont'd)

(4) Pulse Count Timing

Table 6.4 External Input Pulse Count Timing

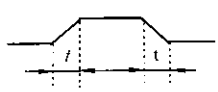
Pulse Input Mode	Pulse Count Mode	ADD	SUBTRACT
Phases A and B	×1		
	×2		
	×4		
Sign + Pulse	×1		

Pulse Waveform



The pulse counting time is influenced by the pulse rise and fall time. The countable waveform is as follows:

50kpps t < 2μs
5kpps t <20μs



6.3 PRECAUTIONS FOR I/O TERMINAL CONNECTION AND WIRING

6.3.1 I/O Terminal Connection

(1) TST1 and TST2 Terminal Connection (Example)

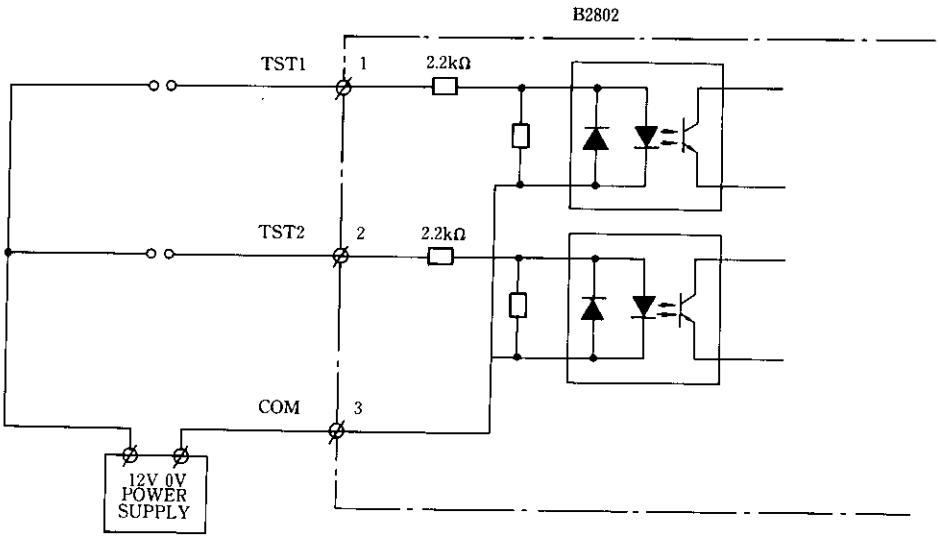


Fig. 6.2 TST1 and TST2 Connection Example

(2) Phases A/B Pulse Input Terminal Connection (Example)

① When the pulse generator is open corrector output (12V)

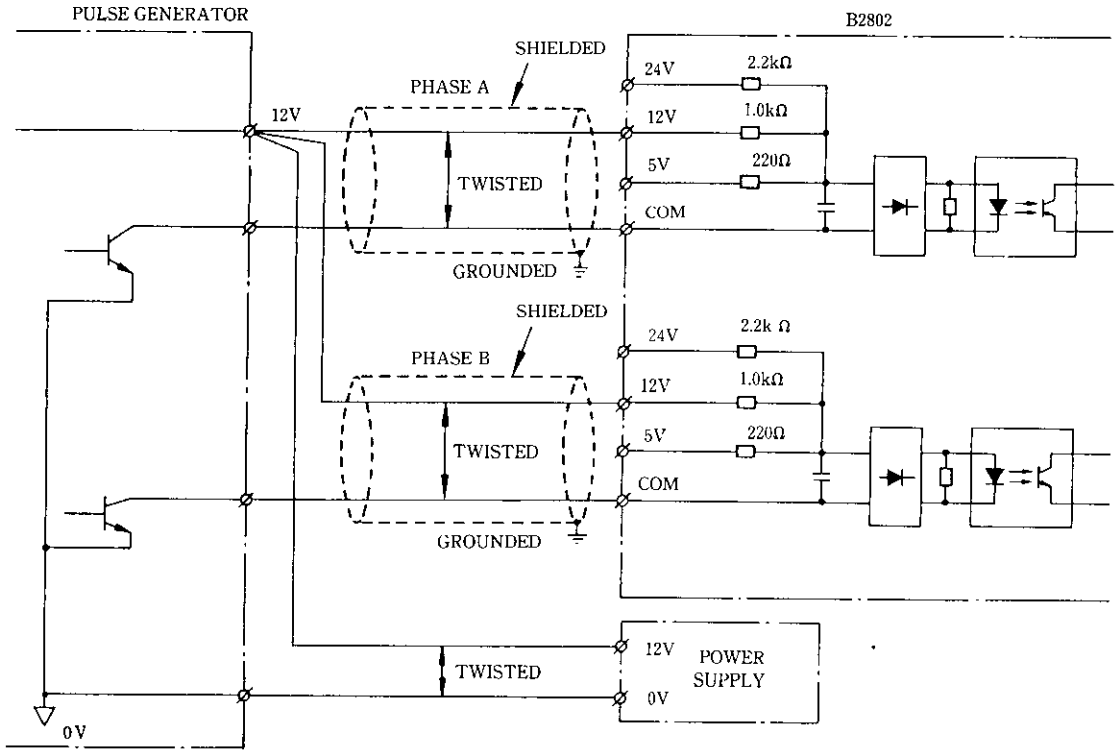


Fig. 6.3 When Pulse Generator is Open Corrector Output (12V)

6.3.1 I/O Terminal Connection (Cont'd)

② When the pulse generator is source voltage output (5V)

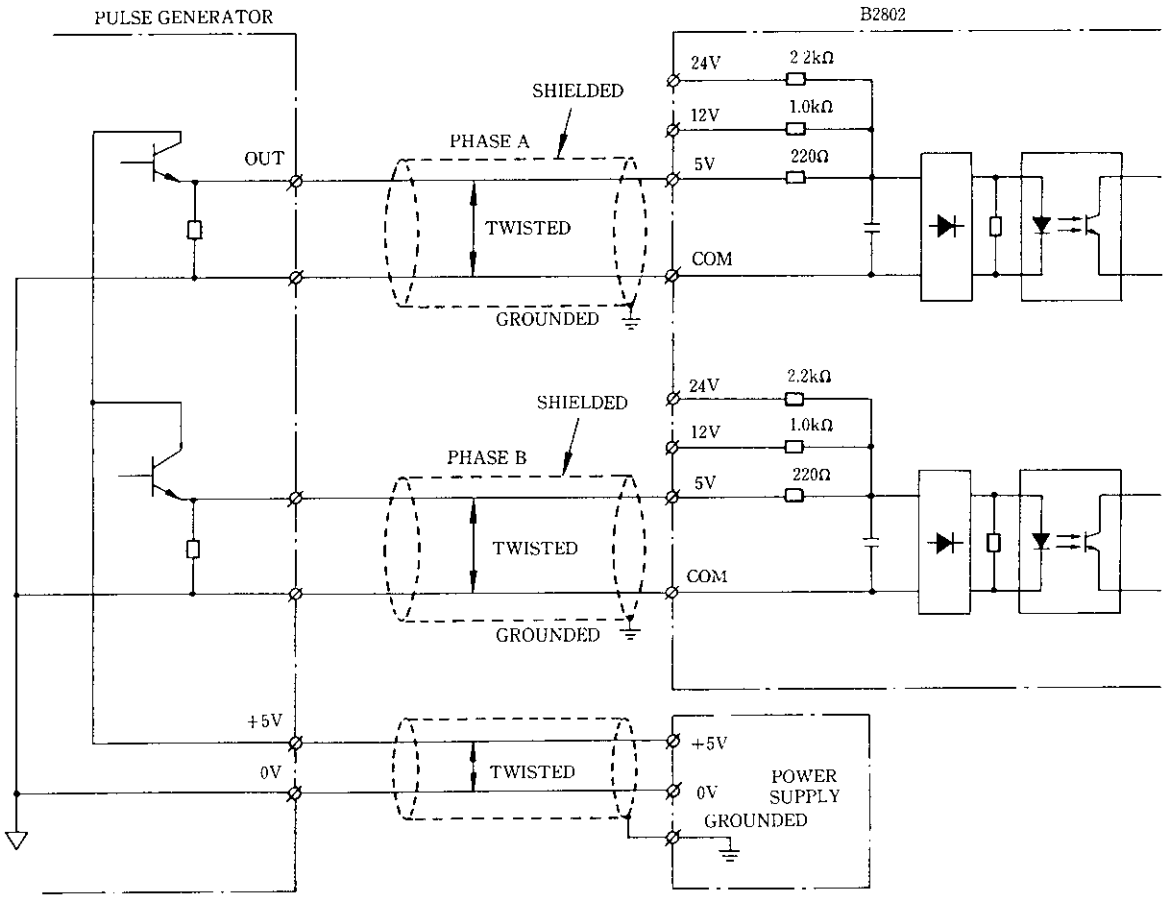


Fig. 6.4 When Pulse Generator is Source Voltage Output (5V)

(3) ENB (External Count Enable) Terminal Connection (Open Corrector 5V) (Example)

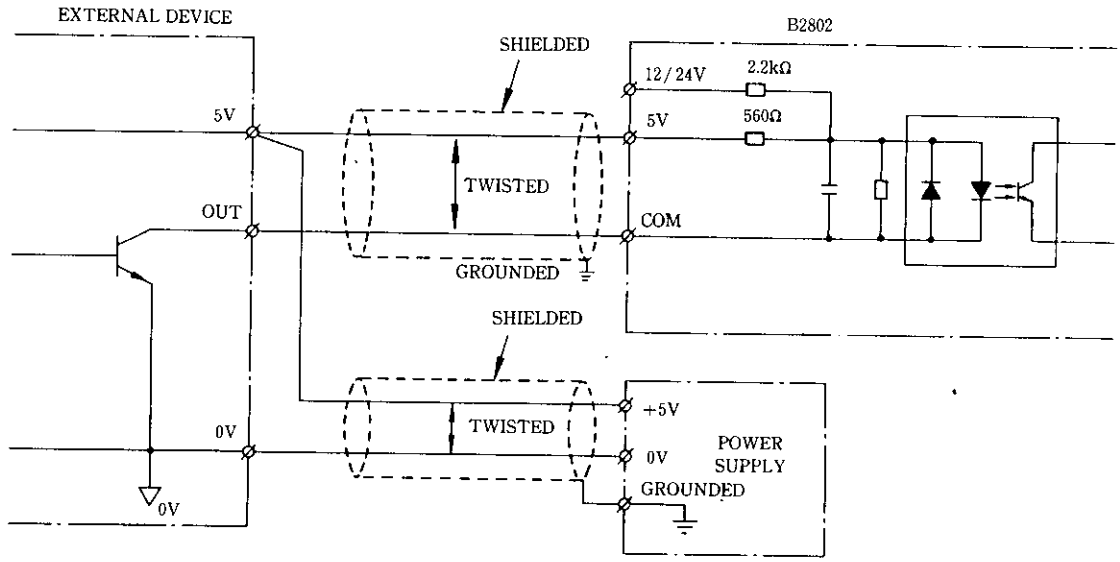


Fig. 6.5 ENB (External Count Enable Input) Terminal Connection Example

(4) RST (External Reset Input) Terminal Connection (Open Corrector 24V) Example

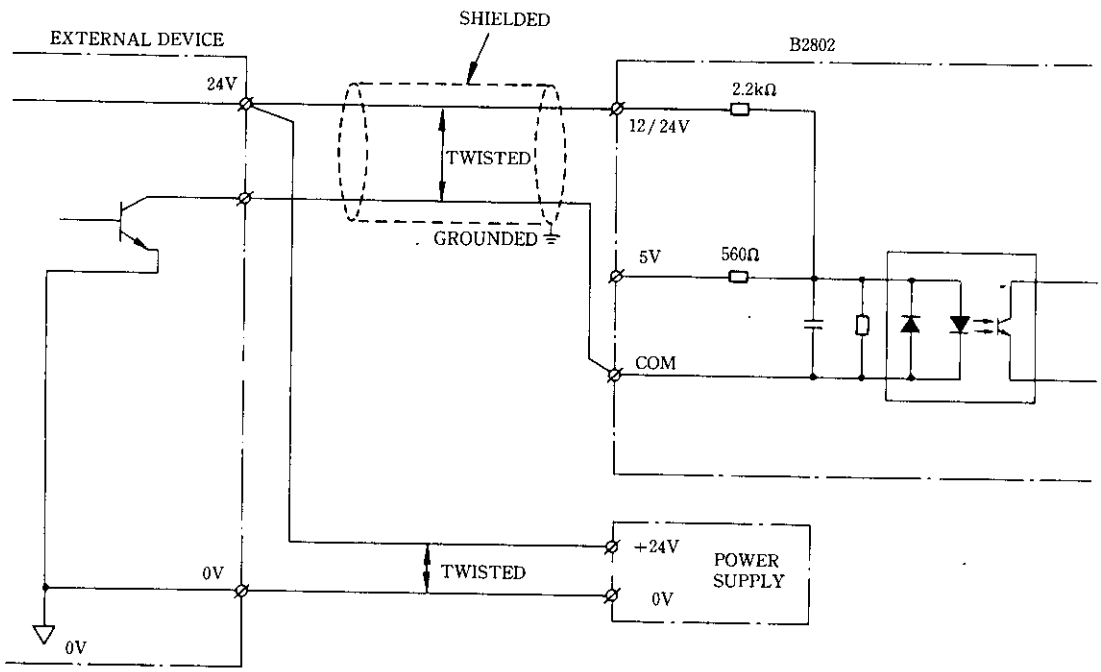


Fig. 6.6 RST (External Reset Input) Terminal Connection Example

6.3.1 I/O Terminal Connection (Cont'd)

(5) External Notch Output Connection (Inductive Load) (Example)

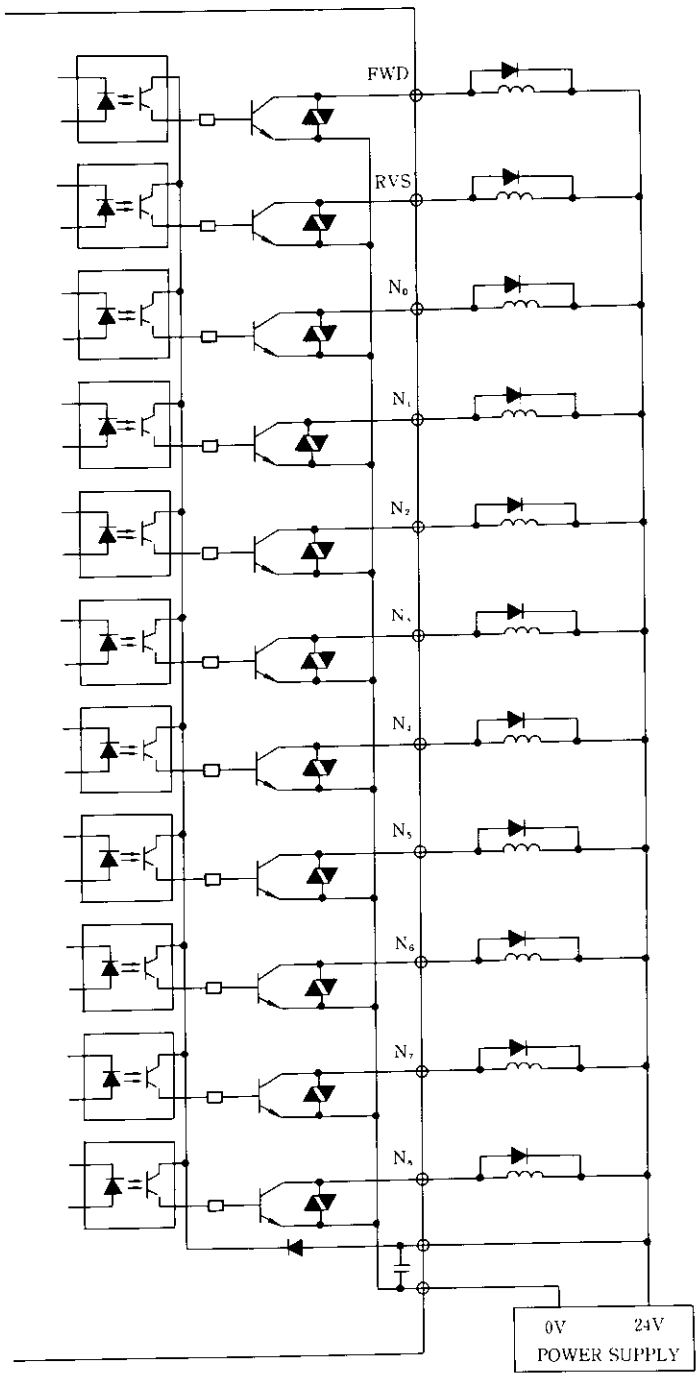


Fig. 6.7 External Notch Output Connection Example (Inductive Load)

6.3.2 Wiring Precautions

(1) Make sure to use shielded twisted pair wires for signal lines.

(2) 30m (100 feet) at 50kpps is a reference wire length. The shorter the better.

(3) Ground the shielding at a single point.

(4) To avoid interference by noise, take the following measures:
- Insert surge killers in coils for relays, contacts and solenoids.
- Provide separation of at least 30cm (one foot) between power lines (AC line, I/O lines) and DC signal lines. Never bundle them together or run them in the same duct.

(5) External Power Supply:
- For external power supply, use general DC stabilized power supply.
- Provide line filter at the AC input side of the DC stabilized power supply, so that primary and secondary sides of line filter and DC output side are not run in the same duct.

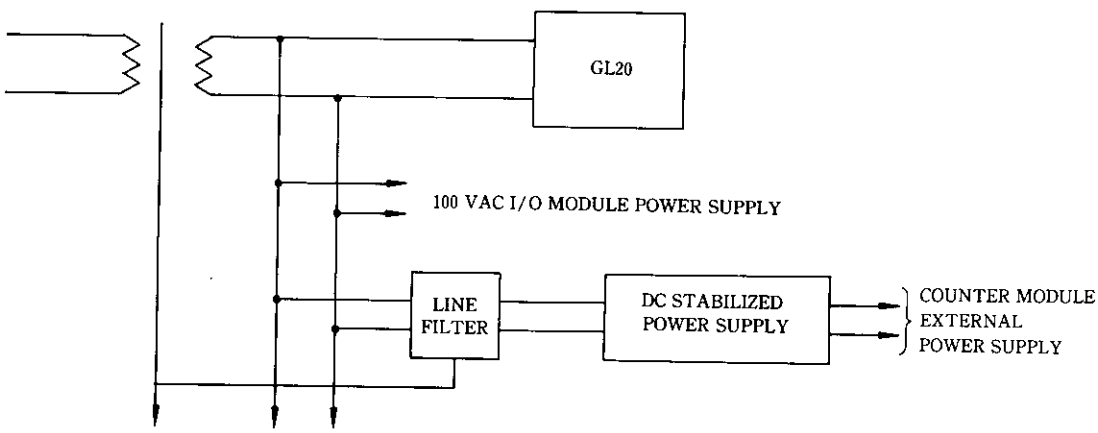


Fig. 6.8 Counter Module External Power Supply

6.4 INDICATORS

Table 6.5 shows the ON conditions for LED indicators.

Table 6.5 LED Indicators

Name	Description
RDY	Indicates result of module self-diagnosis(linked with input relay"READY")
ENB	Lights under the count enable state (when external input "ENB" is ON and and output coil "count enable" is ON.)
PHA	Lights when a signal is fed to phase A.
PHB	Lights when a signal is fed to phase B.
INC	Lights during ADD count.
DEC	Lights during SUBTRACT count.
ERR	Lights when preset error or scan time error occurs.
FWD	Lights while external forward run output is ON.
RVS	Lights while external reverse run output is ON.
N_0	Lights while external notch output 0 is ON.
N_1	Lights while external notch output 1 is ON.
N_2	Lights while external notch output 2 is ON.
N_3	Lights while external notch output 3 is ON.
N_4	Lights while external notch output 4 is ON.
N_5	Lights while external notch output 5 is ON.
N_6	Lights while external notch output 6 is ON.
N_7	Lights while external notch output 7 is ON.
N_8	Lights while external notch output 8 is ON.

Note:
1. ENB is OFF at the test mode and conter resetting ("EXTERNAL RESET" ON or "CURRENT COUNT RESET" ON)
2. PRESET ERROR remains ON until the normal value is set.

7. TEST RUN

7.1 PRECAUTIONS BEFORE TEST RUN

Before turning the power on check wiring and connections.

(1) Are the switch setting correct for the CPU module ?

(2) Is the voltage level of the B2802 input terminals correctly set ?
Wrong wiring may damage the units.

(3) Is wiring for each terminal correct ?

7.2 POWER ON

(1) After switch settings of the B2802 and wiring are checked correct, turn the power switch on.

RDY lights when self-diagnosis of the module is completed without any trouble.

(2) Operate the pulse generator.

PHA and PHB blink for "phase A/B pulse" inputs. PHA blinks for "sign + pulse" input.

(3) Verify whether directions of ADD/SUBTRACT by the pulse generator and that of B2802 coincide by INC and DEC.

- Set the counter to "count enable." ENB should light.
- Operate the pulse generator. INC should light for ADD direction and DEC should light for SUBTRACT direction.

8. TROUBLESHOOTING

8.1 SELF DIAGNOSIS OF B2802

(1) Self diagnosis of the B2802 include the following:

① During power up
- ROM total sum check
- RAM check

② During operation
- ROM total sum check
- WDT check
- Various setting errors
- Monitoring of CPU module scan time
- RUN/STOP status check of CPU module

(2) Corrective Action for Errors

Table 8.1 shows error symptoms and required corrective action.

Table 8.1 Error Displays and Corrective Action

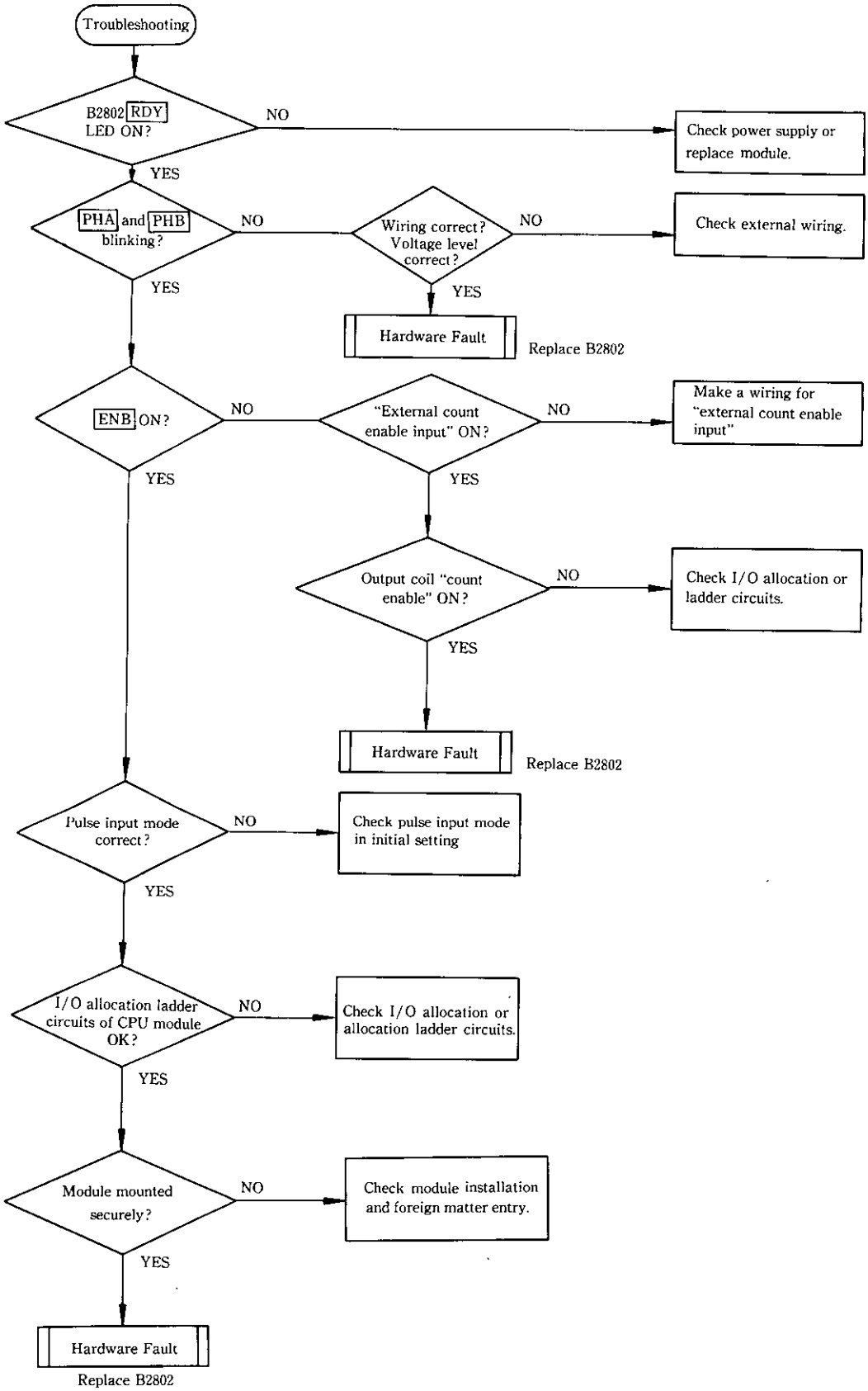
ERROR	Input Relay		LED Indicator		External	Corrective Action
	READY	Scan Time Error	RDY	ERR	Output	
ROM/RAM Check Error, WDT Error	OFF	OFF	OFF	OFF	OFF	Reset the module or turn the internal power supply OFF and then ON again. If the same errors are found, replace the B2802.
Setting Error	ON	OFF	ON	ON	Normal	Perform correct settings.
Service Scan Time of CPU Module is too Short	ON	ON	ON	ON	Normal	This error occurs when very few if any, ladder circuits are stored in the CPU module. Add more ladder circuits or dummy allocations.

When a CPU module is stopped by the programming panel, the external outputs (FWD, RVS, notch outputs 0 to 8) become OFF, but the count continues. Therefore, when the CPU module is started again and counter current count may change, resulting in change of the external output.

8.2 SYSTEM TROUBLESHOOTING

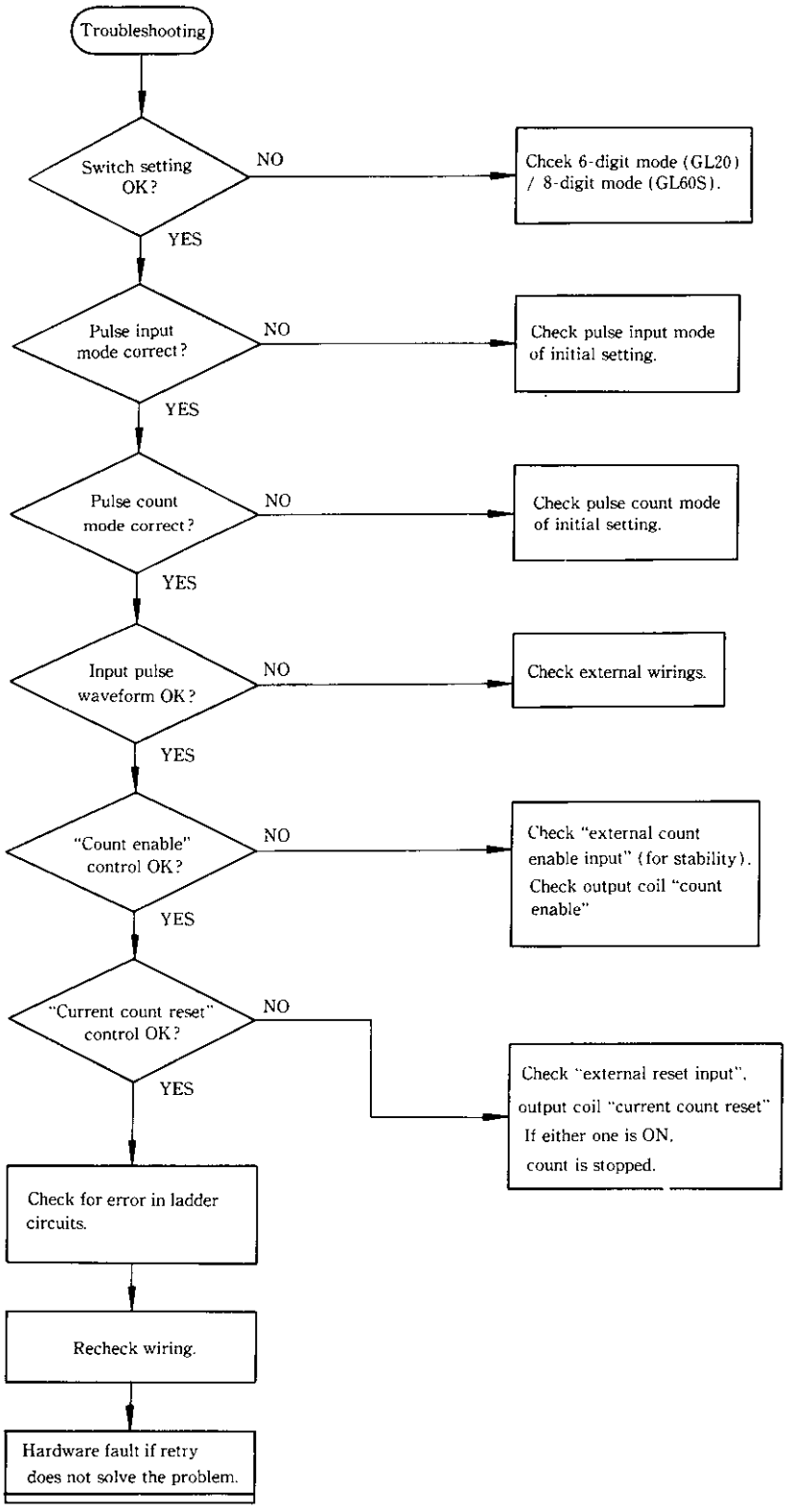
When a fault occurs, first, check if it is due to faulty manipulation or to system defects.

(1) B2802 does not count

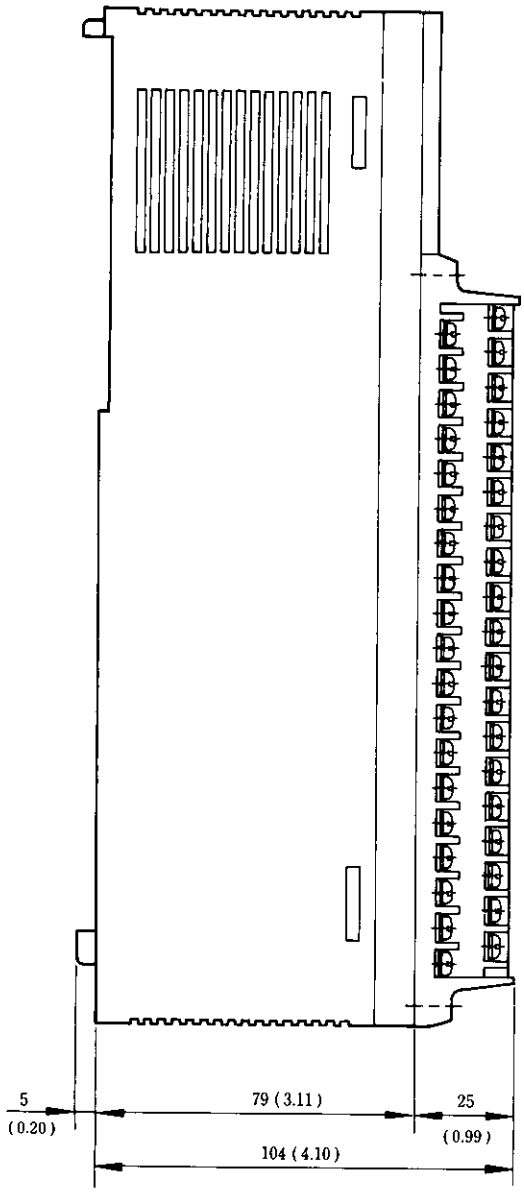


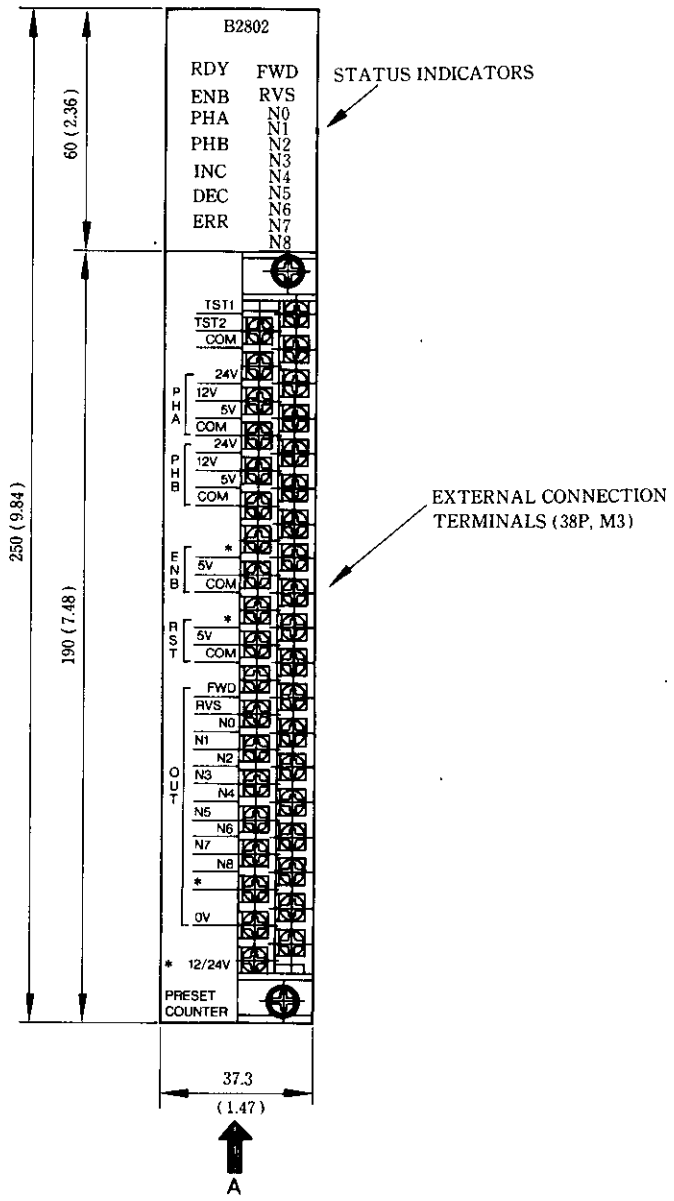
8.2 SYSTEM TROUBLESHOOTING (Cont'd)

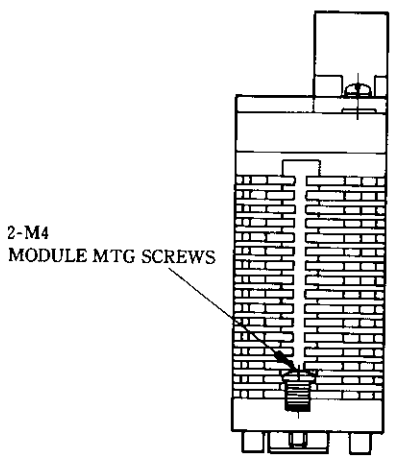
(2) B2802 Counts but Wrong



9. DIMENSIONS in mm (inches)







View A

Approx. Weight : 0.6kg (1.3 lb)

APPENDIX INTERNAL INTERFACE SIGNAL LIST

Table A1 Output Coil List

GL20	GL60S	Signal Name
0001 + 8n	00001 + 8n	Module reset
0002 + 8n	00002 + 8n	Initial setting
0003 + 8n	00003 + 8n	Current count reset
0004 + 8n	00004 + 8n	Count enable
0005 + 8n	00005 + 8n	Output enable
0006 + 8n	00006 + 8n	Current count preset command
0007 + 8n	00007 + 8n	Notch point preset command
0008 + 8n	00008 + 8n	Forward run output
0009 + 8n	00009 + 8n	Reverse run output
0010 + 8n	00010 + 8n	Forced notch output 0
0011 + 8n	00011 + 8n	Forced notch output 1
0012 + 8n	00012 + 8n	Forced notch output 2
0013 + 8n	00013 + 8n	Forced notch output 3
0014 + 8n	00014 + 8n	Forced notch output 4
0015 + 8n	00015 + 8n	Forced notch output 5
0016 + 8n	00016 + 8n	Forced notch output 6
0017 + 8n	00017 + 8n	Forced notch output 7
0018 + 8n	00018 + 8n	Forced notch output 8
0019 + 8n	00019 + 8n	Monitor 0
0020 + 8n	00020 + 8n	Monitor 1
0021 + 8n	00021 + 8n	Monitor 2
0022 + 8n	00022 + 8n	Monitor 3
0023 + 8n	00023 + 8n	Reserved for future use
0024 + 8n	00024 + 8n	Reserved for future use

For the 16-point allocation, these signals are treated as OFF in the module.

n=0, 1, 2····

Reference Nos. for Output Coil Allocation

Table A2 Input Relay List

GL20	GL60S	Signal Name
0001 + 8n	10001 + 8n	READY
0002 + 8n	10002 + 8n	Preset ACK
0003 + 8n	10003 + 8n	Preset NAK
0004 + 8n	10004 + 8n	Carry
0005 + 8n	10005 + 8n	Borrow
0006 + 8n	10006 + 8n	Notch output 0
0007 + 8n	10007 + 8n	Notch output 1
0008 + 8n	10008 + 8n	Notch output 2
0009 + 8n	10009 + 8n	Notch output 3
0010 + 8n	10010 + 8n	Notch output 4
0011 + 8n	10011 + 8n	Notch output 5
0012 + 8n	10012 + 8n	Notch output 6
0013 + 8n	10013 + 8n	Notch output 7
0014 + 8n	10014 + 8n	Notch output 8
0015 + 8n	10015 + 8n	Reserved for future use
0016 + 8n	10016 + 8n	Scan time error

n=0, 1, 2····

Reference Nos. for Input Relay Allocation

Table A3 Output Register Allocations

GL20	GL60S	Output Register No.
4001 + n	40001 + n	1ST
4002 + n	40002 + n	2ND
4003 + n	40003 + n	3RD
4004 + n	40004 + n	4TH
4005 + n	40005 + n	5TH
4006 + n	40006 + n	6TH
4007 + n	40007 + n	7TH
4008 + n	40008 + n	8TH

2 Registers Allocated

8 Registers Allocated

n=0, 1, 2 ····

Reference Nos. for Output Register Allocations

Table A4 Initial Values Setting to Output Registers

(GL20 [ ][ ][ ] (3 Digits), GL60S [ ][ ][ ][ ] (4 Digits))

1ST

0	0	0	0

PULSE INPUT MODE SETTING
- 0 : SIGN + PULSE
- 1 : PHASE A / B

PHASE A / B PULSE INPUT MODE SETTING
- 0 : 1 MULTIPLIER
- 1 : 2 MULTIPLIERS
- 2 : 4 MULTIPLIERS

(WHEN SIGN + PULSE INPUT IS DESIGNATED, ONE MULTIPLIER IS SELECTED AUTOMATICALLY. THIS POSITION IS SKIPPED.)

NOTCH OUTPUT MODE SETTING
- 0 : PATTERN A
- 1 : PATTERN B

2ND

0	0	0	0

HYSTERESIS WIDTH SETTING
0 TO 99 PULSES

NOTCH POINT SETTING MODE
- 0 : 1-NOTCH POINT SETTING (2 OUTPUT REGISTERS × 1 SCAN)
- 1 : 4-NOTCH POINT SETTING (2 OUTPUT REGISTERS × 2 SCANS)
- 2 : 4-NOTCH POINT SETTING (8 OUTPUT REGISTERS × 1 SCAN)
- 3 : 8-NOTCH POINT SETTING (2 OUTPUT REGISTERS × 8 SCANS)
- 4 : 8-NOTCH POINT SETTING (8 OUTPUT REGISTERS × 2 SCANS)

< Precautions in Initial Setting Process >

(a) When the initial setting is made:
- Counter current count is cleared.
- Notch point preset values are cleared and all notch outputs are turned OFF.
- The current count preset value is cleared.
- Preset errors are cleared.

(b) The initial setting items are checked for normal/abnormal value item by item. When abnormal values are set, the old setting remains for those items, and other items are replaced by the new set values. At this time, PRESET NAK turns ON.

(c) Unused digit places are idle, and on the monitor, idle data is indicated.

Table A5 Input Register Allocations

GL20	GL60S	Input Register No.
3001 + n	30001 + n	1ST
3002 + n	30002 + n	2ND

n=0, 1, 2 ····

Reference Nos. for Input Register Allocations

A Better Tomorrow for Industry through Automation

YASKAWA Electric Mfg. Co., Ltd.

TOKYO OFFICE Ohtemachi Bldg., 1-6-1 Ohtemachi, Chiyoda-ku, Tokyo, 100 Japan
Phone (03) 284-9111, -9145 Telex YASKAWA J33530 Fax (03) 284-9034

SEOUL OFFICE Seoul Center Bldg., 91-1, So Kong-Dong, Chung-Ku, Seoul, Korea
Phone (02) 776-7844 Fax (02) 753-2639

SINGAPORE OFFICE CPF Bldg., 79 Robinson Road No. 24-03, Singapore 0106
Phone 2217530 Telex (87) 24890 YASKAWA RS Fax (65) 224-5854

TAIPEI OFFICE Union Commercial Bldg., 137, Nanking East Road, Sec. 2, Taipei, Taiwan
Phone (02) 507-7065,-7732 Fax (02) 506-3837

YASKAWA ELECTRIC AMERICA, INC.: SUBSIDIARY

Chicago Office (Head Office) 3160 MacArthur Blvd.,Northbrook, Illinois 60062-1917,U.S.A.
Phone (312) 291-2340 Telex (230) 270197 YSKW YSNC NBRK Fax (312) 498-2430, 480-9731

Los Angeles Office 7341 Lincoln Way, Garden Grove, California 92641, U.S.A.
Phone (714) 894-5911 Telex (230) 678396 YASKAWAUS TSTN Fax (714) 894-3258

New Jersey Office 30 Two Bridges Road, Fairfield, New Jersey 07006, U.S.A.
Phone (201) 575-5940 Fax (201) 575-5947

YASKAWA ELECTRIC EUROPE GmbH: SUBSIDIARY
Monschauerstrasse 1, 4000 Düsseldorf 11, West Germany
Phone (0211) 501127 Telex (41) 8588673 YASD D Fax (0211) 507737

YASKAWA ELÉTRICO DO BRASIL COMÉRCIO LTDA.: SUBSIDIARY
Av. Brig. Faria Lima, 1664-cj. 721/724, Pinheiros, São Paulo-SP, Brasil CEP-01452
Phone (011) 813-3933, 813-3694 Telex (011) 82869 YSKW BR

Due to ongoing product modification/improvement, data subject to change without notice.

 89-8-6.0 1T